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(54) **GRAPHICS PIPELINE TOKEN SYNCHRONIZATION**

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(52) **U.S. Cl.** **345/506**; 345/522; 345/501; 345/502

(58) **Field of Search** 345/506, 522, 345/422, 501–505, 556; 712/40, 219

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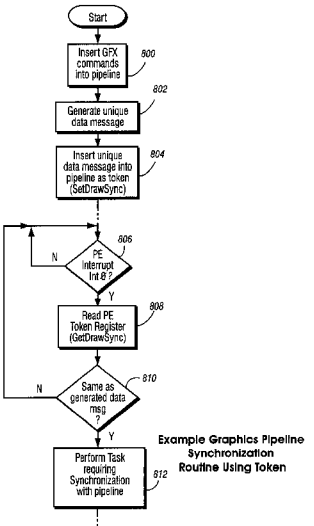
(57) **ABSTRACT**

A graphics system including a custom graphics and audio processor produces exciting 2D and 3D graphics and surround sound. The system includes a graphics and audio processor including a 3D graphics pipeline and an audio digital signal processor. The graphics pipeline processes graphics commands at different rates depending upon the type of operation being performed. This makes it difficult to synchronize pipeline operations with external operations (e.g., a graphics processor with a main processor). To solve this problem, a synchronization token including a programmable data message is inserted into a graphics command stream sent to a graphics pipeline. At a predetermined point near the bottom of the pipeline, the token is captured and a signal is generated indicated the token has arrived. The graphics command producer can look at the captured token to determine which of multiple possible tokens has been captured, and can use the information to synchronize a task with the graphics pipeline. Applications include maintaining memory coherence in memory shared between the 3D graphics pipeline and a graphics command producer.

17 Claims, 8 Drawing Sheets



Example Graphics Pipeline Synchronization Routine Using Token

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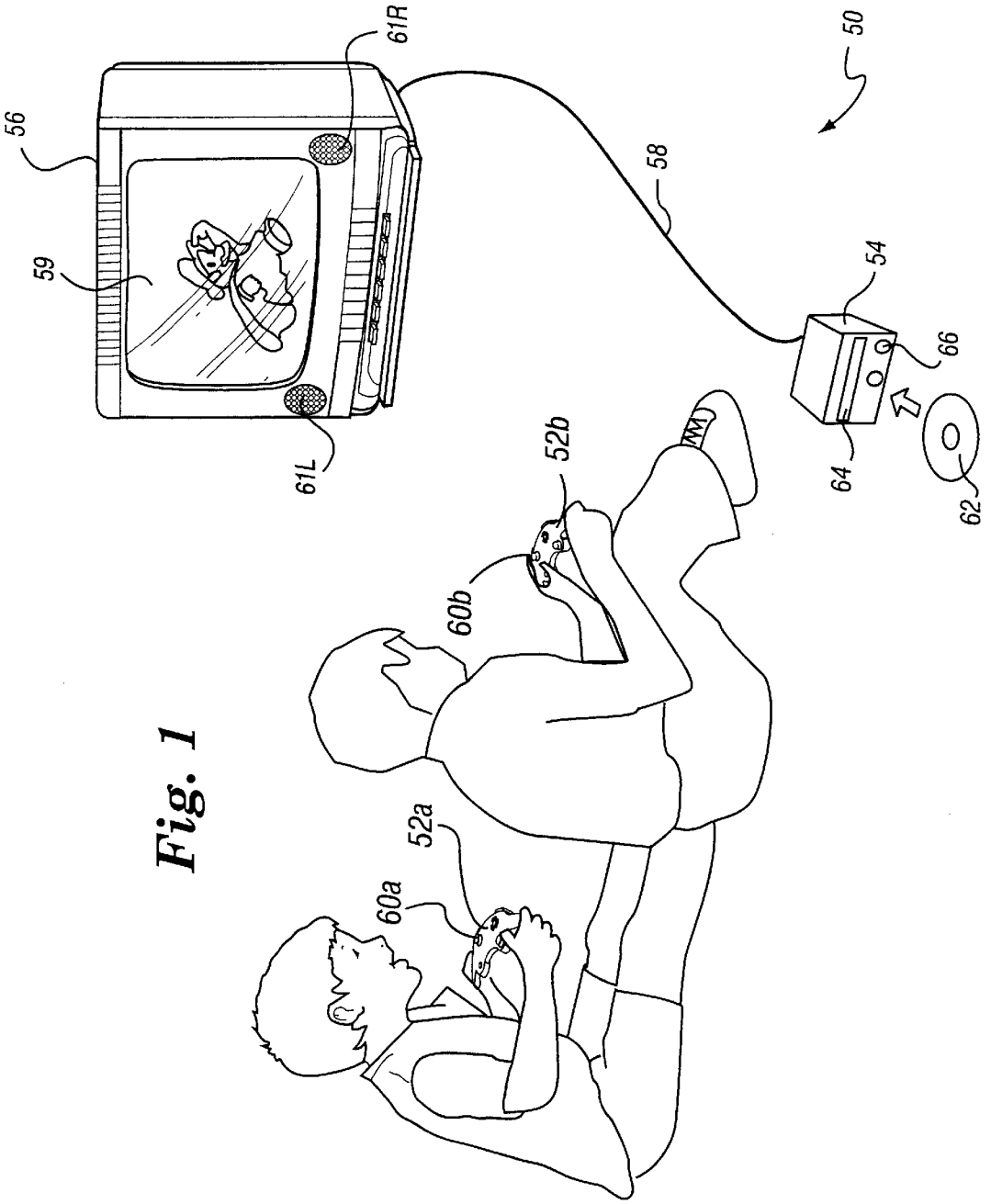

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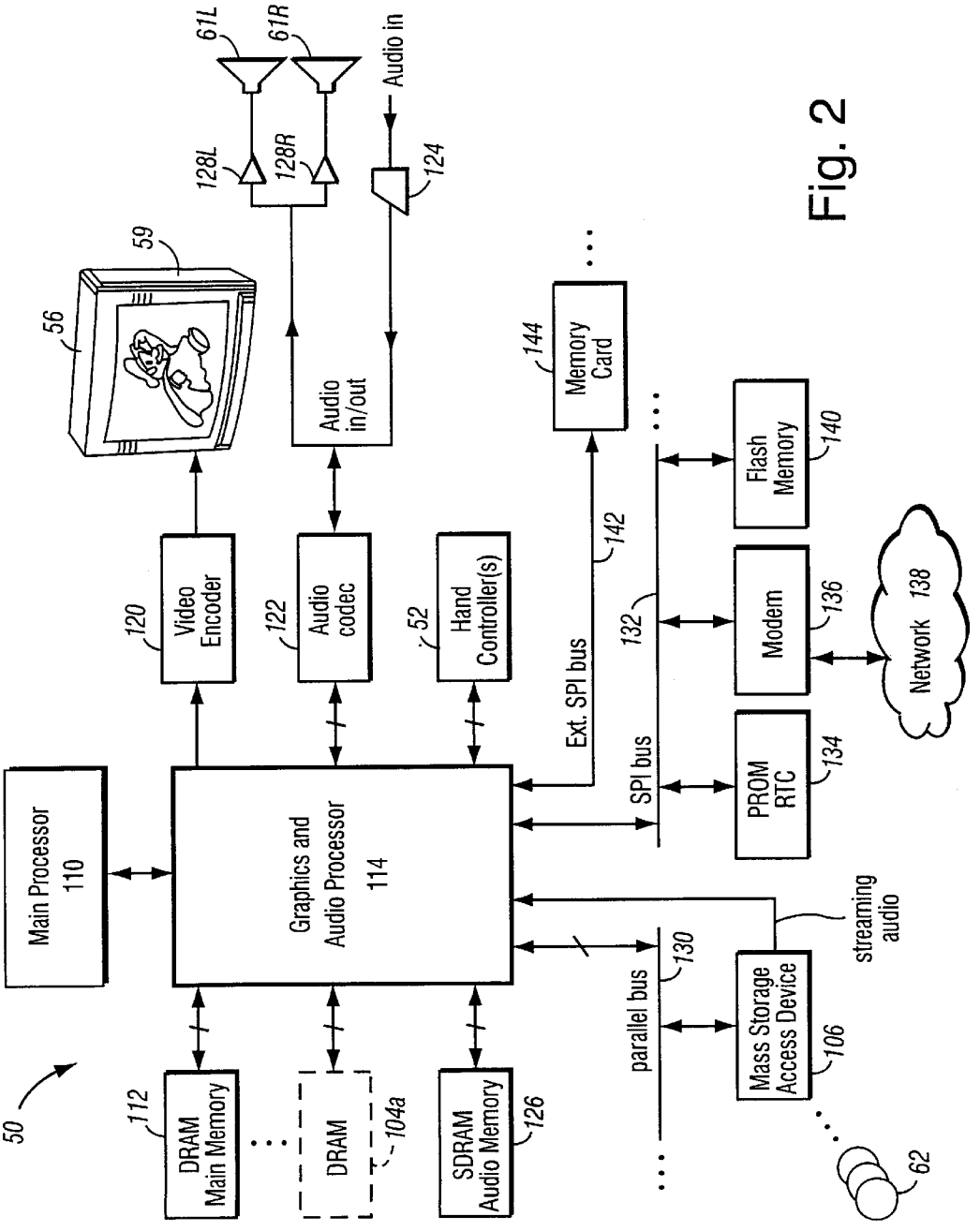
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Graphics and Audio Processor 114
DRAM Main Memory 112
DRAM 104a
SDRAM Audio Memory 126
Video Encoder 120
Audio codec 122
Hand Controller(s) 52
Audio in/out
61L
61R
128L
128R
Audio in
124
59
56
Ext. SPI bus 142
SPI bus 132
parallel bus 130
Memory Card 144
Flash Memory 140
Modem 136
PROM RTC 134
Mass Storage Access Device 106
streaming audio
Network 138
62

Fig. 2

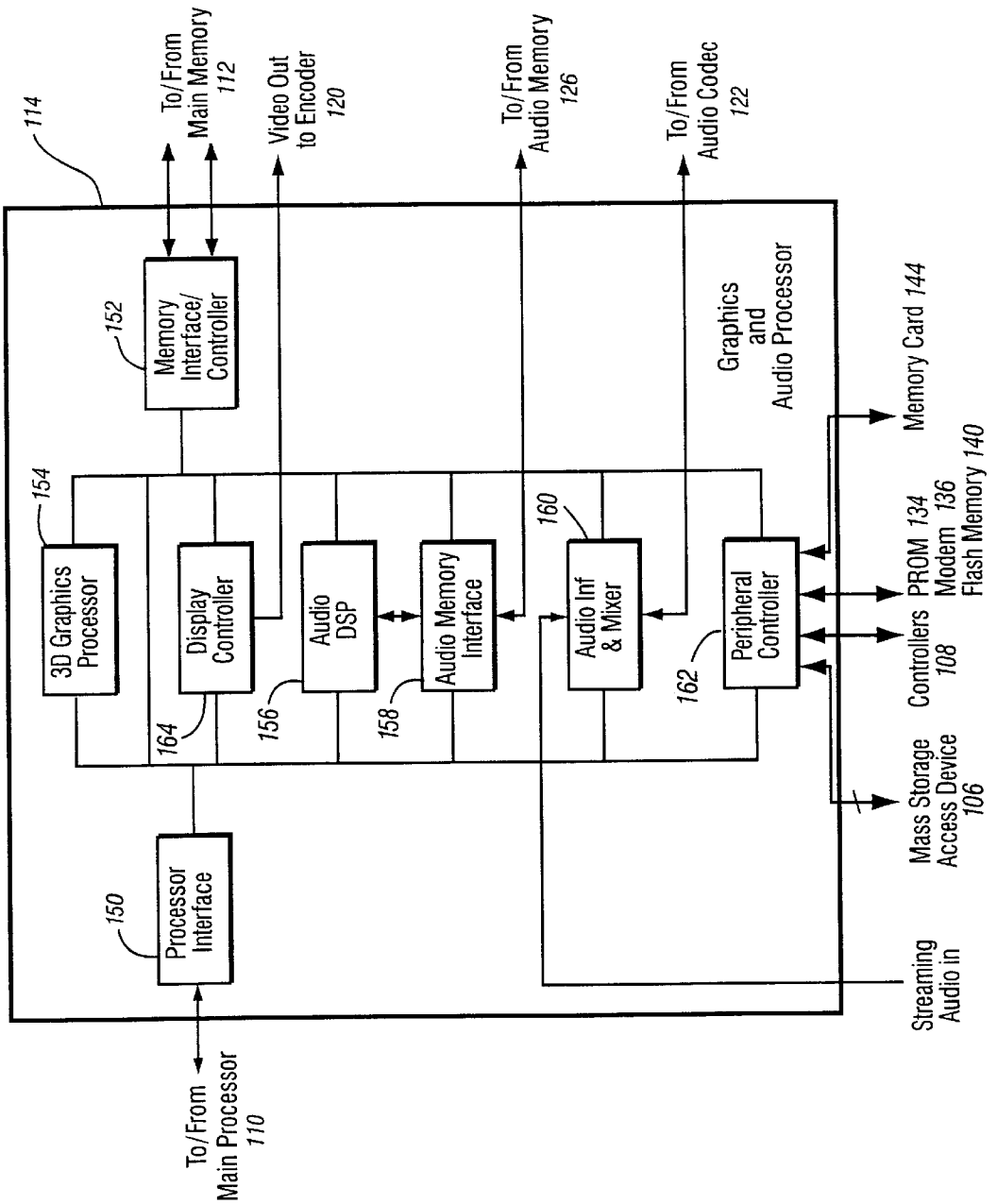

114
To/From Main Memory 112
Video Out to Encoder 120
To/From Audio Memory 126
To/From Audio Codec 122
Memory Interface/ Controller
152
Graphics and Audio Processor
3D Graphics Processor
154
Display Controller
164
Audio DSP
156
Audio Memory Interface
158
Audio Inf & Mixer
160
Peripheral Controller
162
Processor Interface
150
Memory Card 144
PROM 134
Modem 136
Flash Memory 140
Controllers 108
Mass Storage Access Device 106
Streaming Audio in
To/From Main Processor 110

Fig. 3

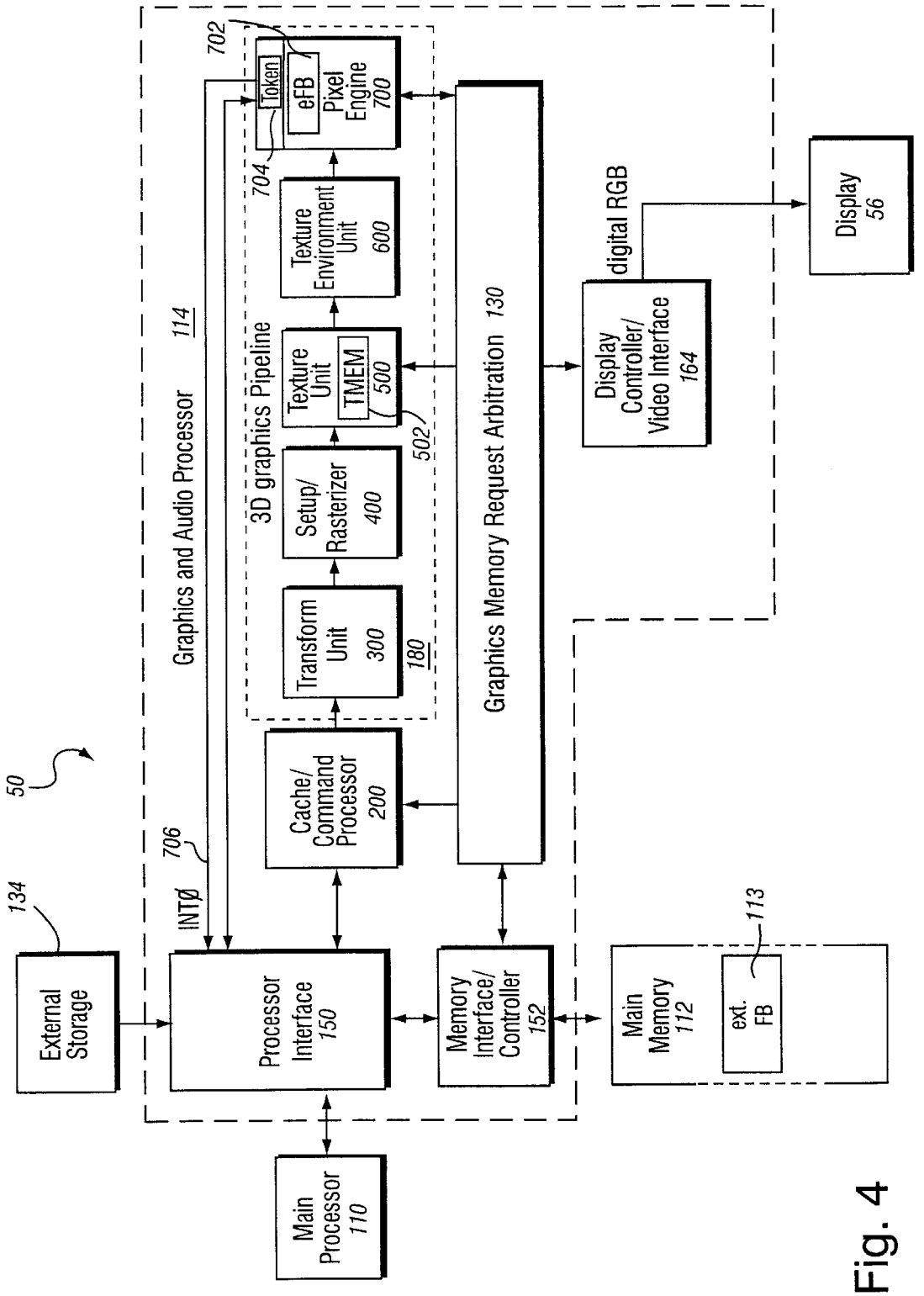

50
Graphics and Audio Processor 114
3D graphics Pipeline
180
Transform Unit 300
Setup/ Rasterizer 400
Texture Unit 500
TMEM
Texture Environment Unit 600
Token
eFB
Pixel Engine 700
702
704
706
INTØ
Cache/ Command Processor 200
Graphics Memory Request Arbitration 130
Display Controller/ Video Interface 164
digital RGB
Display 56
External Storage 134
Processor Interface 150
Memory Interface/ Controller 152
Main Memory 112
ext. FB
113
Main Processor 110

Fig. 4

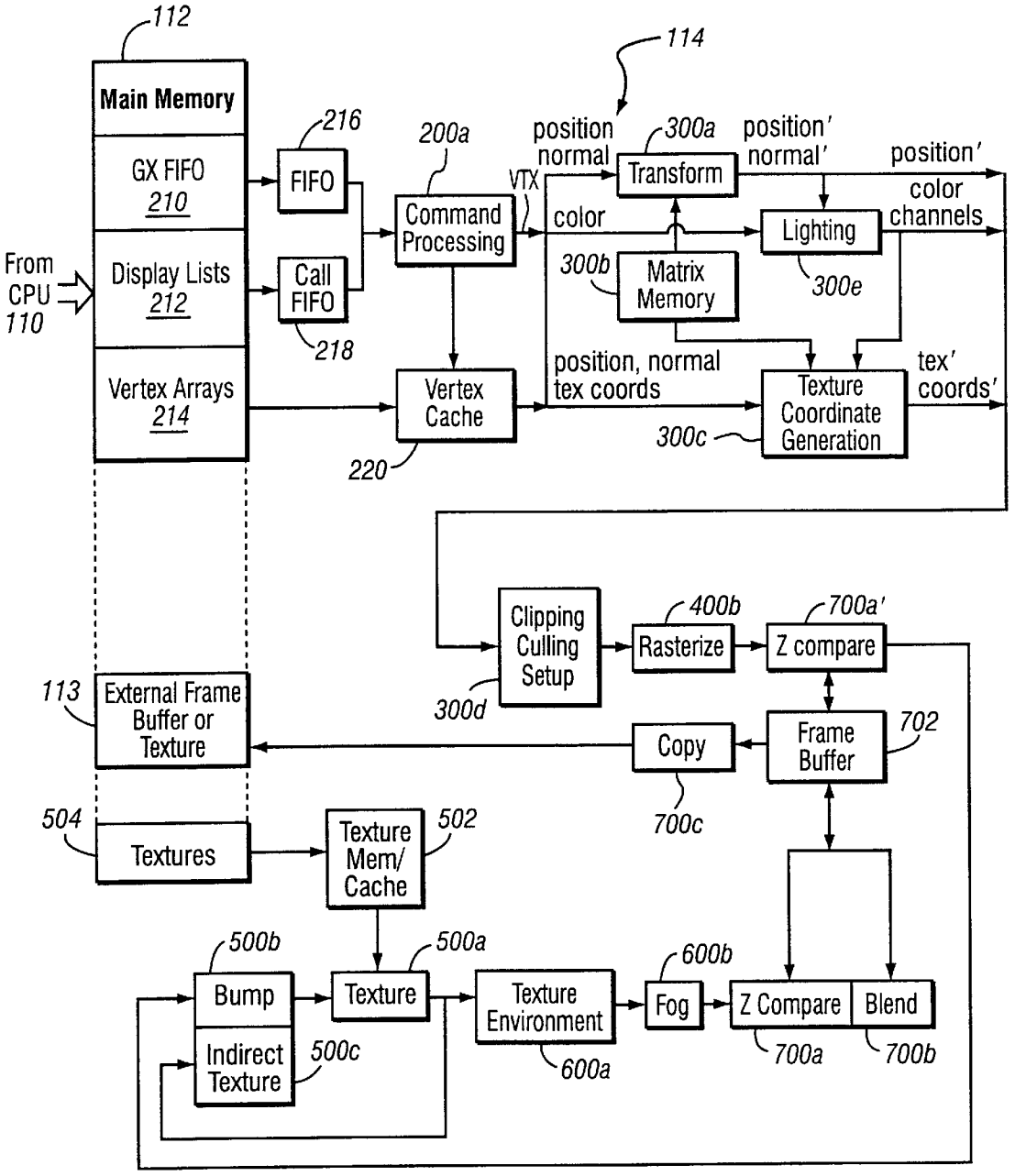
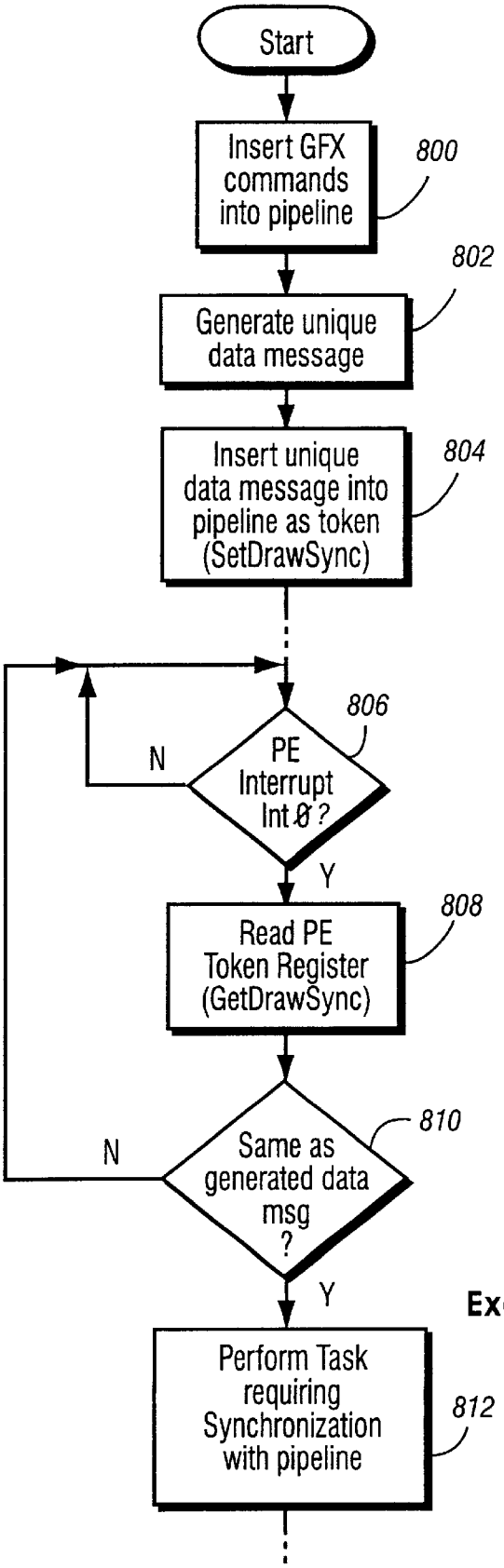


Fig. 5 EXAMPLE GRAPHICS PROCESSOR FLOW



Example Graphics Pipeline Synchronization Routine Using Token

Fig. 6

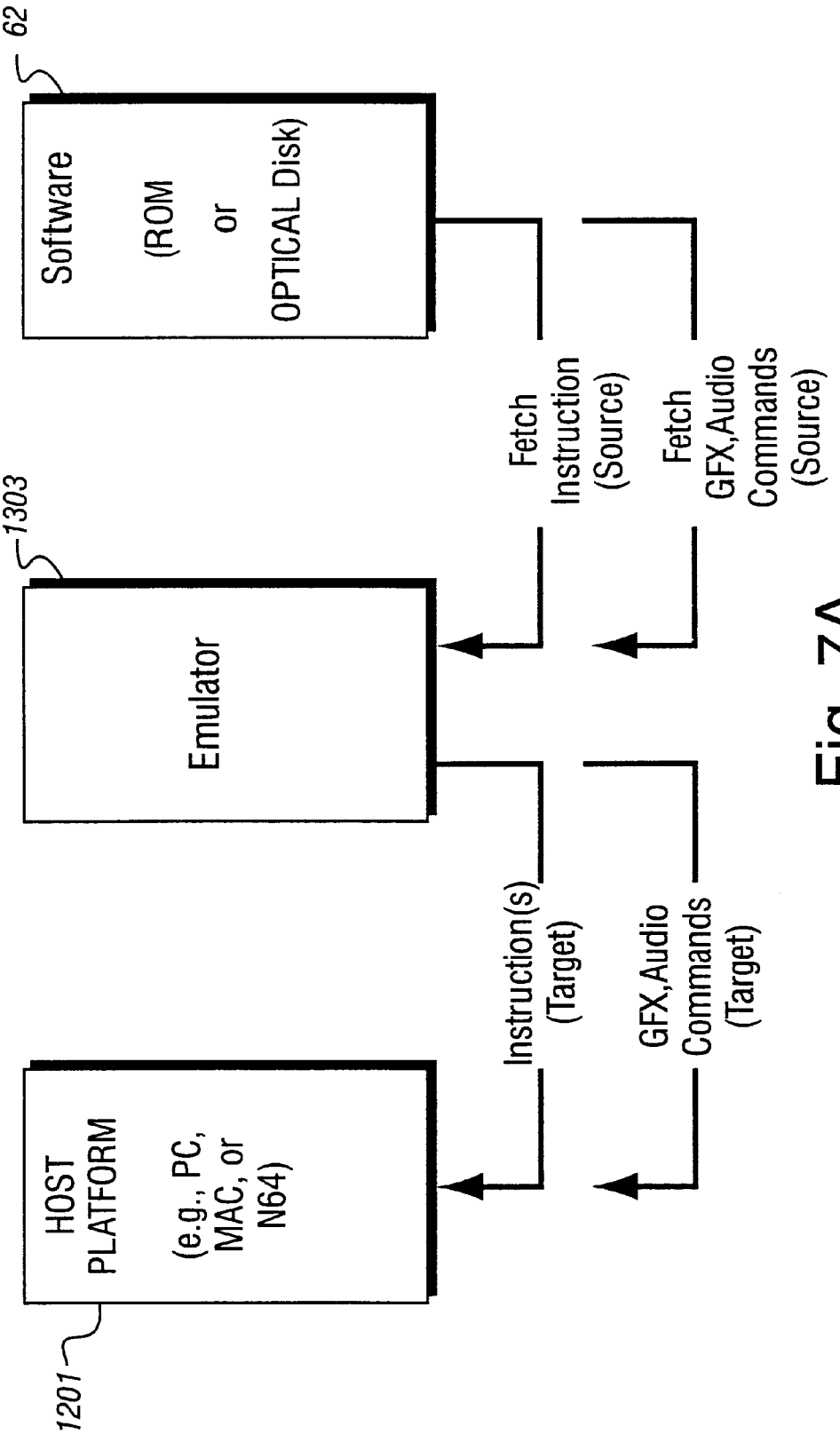

62
Software
(ROM
or
OPTICAL Disk)
1303
Emulator
1201
HOST
PLATFORM
(e.g., PC,
MAC, or
N64)
Fetch
Instruction
(Source)
Fetch
GFX,Audio
Commands
(Source)
Instruction(s)
(Target)
GFX,Audio
Commands
(Target)

Fig. 7A

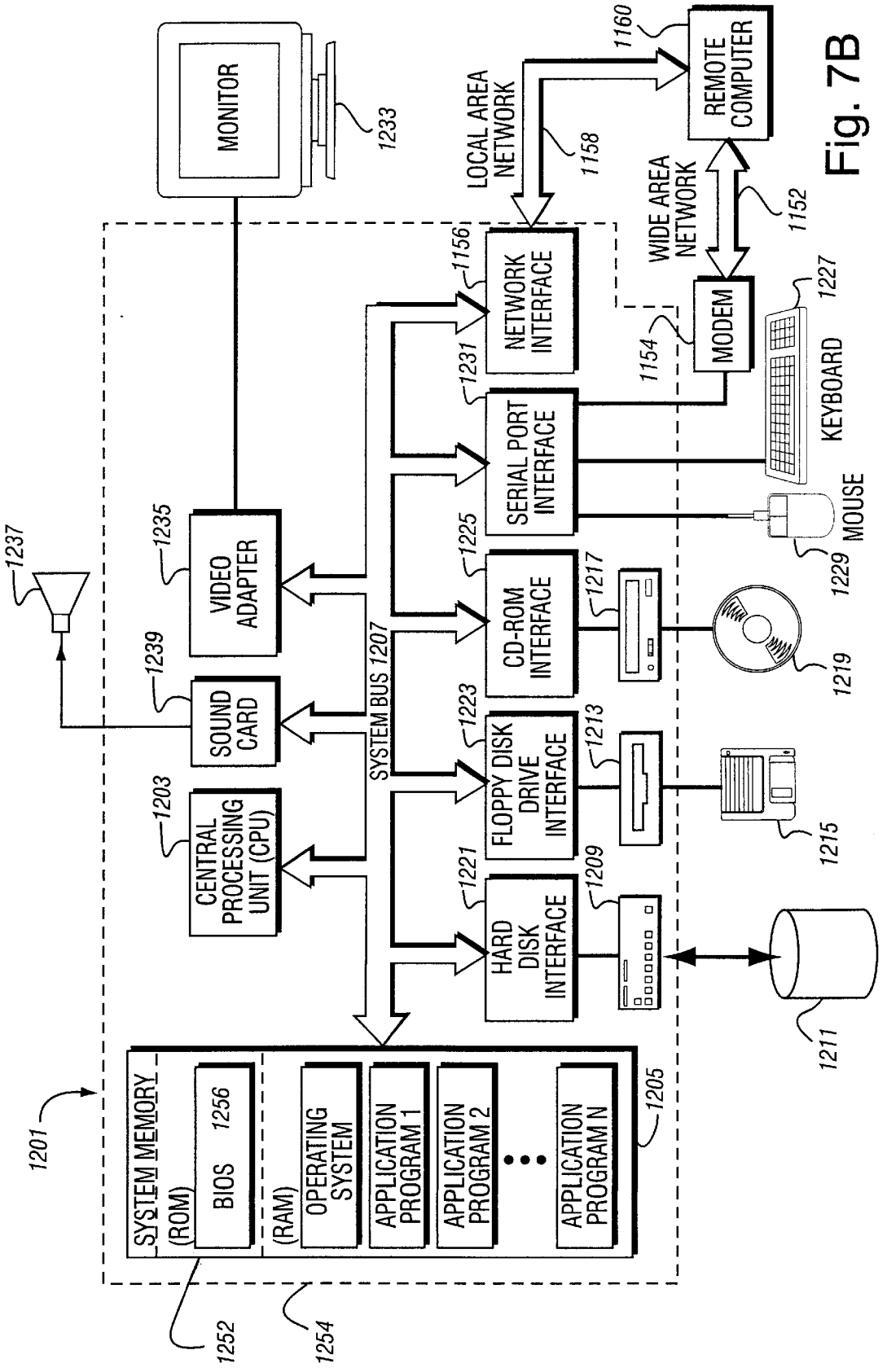

MONITOR
1233
LOCAL AREA NETWORK
1158
1160
REMOTE COMPUTER
WIDE AREA NETWORK
1152
1156
NETWORK INTERFACE
1231
SERIAL PORT INTERFACE
1154
MODEM
1227
KEYBOARD
MOUSE
1229
1225
CD-ROM INTERFACE
1217
1219
1223
FLOPPY DISK DRIVE INTERFACE
1213
1215
1221
HARD DISK INTERFACE
1209
1211
SYSTEM BUS 1207
1235
VIDEO ADAPTER
1237
1239
SOUND CARD
1203
CENTRAL PROCESSING UNIT (CPU)
1201
SYSTEM MEMORY
(ROM)
BIOS 1256
(RAM)
OPERATING SYSTEM
APPLICATION PROGRAM 1
APPLICATION PROGRAM 2
APPLICATION PROGRAM N
1205
1252
1254

Fig. 7B

GRAPHICS PIPELINE TOKEN SYNCHRONIZATION

This application claims the benefit of U.S. Provisional Application No. 60/226,889, filed Aug. 23, 2000, the entire content of which is hereby incorporated by reference in this application.

FIELD OF THE INVENTION

The present invention relates to computer graphics, and more particularly to interactive graphics systems such as home video game platforms. Still more particularly this invention relates to synchronization between a graphics pipeline and a graphics command producer using variable content synchronization tokens.

BACKGROUND AND SUMMARY OF THE INVENTION

Many of us have seen films containing remarkably realistic dinosaurs, aliens, animated toys and other fanciful creatures. Such animations are made possible by computer graphics. Using such techniques, a computer graphics artist can specify how each object should look and how it should change in appearance over time, and a computer then models the objects and displays them on a display such as your television or a computer screen. The computer takes care of performing the many tasks required to make sure that each part of the displayed image is colored and shaped just right based on the position and orientation of each object in a scene, the direction in which light seems to strike each object, the surface texture of each object, and other factors.

Because computer graphics generation is complex, computer-generated three-dimensional graphics just a few years ago were mostly limited to expensive specialized flight simulators, high-end graphics workstations and supercomputers. The public saw some of the images generated by these computer systems in movies and expensive television advertisements, but most of us couldn't actually interact with the computers doing the graphics generation. All this has changed with the availability of relatively inexpensive 3D graphics platforms such as, for example, the Nintendo 64® and various 3D graphics cards now available for personal computers. It is now possible to interact with exciting 3D animations and simulations on relatively inexpensive computer graphics systems in your home or office.

A problem graphics system designers confronted in the past was how to synchronize the graphics pipeline with external components such as the graphics command producer. A typical graphics rendering system consists of several asynchronous components (e.g., graphics command producer that generates graphics commands; the graphics processor consuming the commands and producing frame buffer outputs; and a display interface that displays the frame buffers). It is often desirable to synchronize these different stages of the rendering system to establish time-coherence between various operations. For example, it would be very useful for the graphics command producer to know under certain circumstances when the graphics processor has finished processing a given graphics command. The synchronization problem is complicated in that a typical graphics processor may take different amounts of time to process different graphics commands.

Various solutions to this problem were offered. For example, one technique that has been used in the past to provide synchronization between a graphics pipeline and a graphics command producer is to have the graphics pipeline send an interrupt to the command producer when all of the commands in a graphics display list have been processed. While this synchronization capability is very useful, it does not solve more intermediate synchronization requirements within a graphics display list (e.g., to enable the graphics command producer or other actor to perform some task other than sending new graphics commands while the graphics pipeline continues to work on the remainder of a display list).

It is known to insert variable content token identifiers into a graphics command stream to allow a graphics processor to pick between different items for processing. However, such token identifiers were not generally for synchronization purposes but were used instead to allow the graphics pipeline to identify data structures or other items it was to operate upon.

While significant work has been done in the past, further improvements are desirable.

The present invention solves the synchronization problem by providing techniques and arrangements that synchronize a graphics pipeline with an external actor such as, for example, a graphics command producer. In accordance with one aspect provided by this invention, a token including a variable data message is inserted into a graphics command stream sent to a graphics pipeline. At a predetermined point in the pipeline, the token is captured and a signal is generated indicating a token has arrived. An external device can look at the captured token to determine which of multiple possible tokens has been captured.

In one particular example, the graphics pipeline generates an interrupt when a token arrives at a predetermined point in the pipeline, and the other actor can poll a token register to determine the value of the captured token. The graphics command producer or other actor can use the token synchronization information to synchronize a task with the graphics pipeline, e.g., to maintain memory coherence in memory shared between the graphics pipeline and the graphics command producer. In accordance with another aspect of the invention, the graphics command producer can insert multiple tokens of different values in the same graphics command stream, and use a comparison to determine which token has arrived at the predetermined point in the graphics pipeline. Different tasks can be triggered based on which token has arrived at that point.

In accordance with one aspect provided by the invention, a method of synchronizing with a graphics pipeline comprises sending a variable content synchronization token down the graphics pipeline, and detecting when the token has reached a predetermined point in the pipeline. The token may comprise a variable content data message which, in one embodiment, the graphics pipeline does not modify. The detecting step may comprise comparing a value returned by a token register with a value of the sent token. The detecting step may include polling a token register in response to an interrupt.

In accordance with another aspect provided by this invention, a method of synchronizing with a graphics pipeline of the type including a command processor, a transformation unit, a lighting unit, a texture coordinate generator, a texture mapper, a rasterizer, a blender, a pixel engine and a frame buffer includes inserting a variable content data message into the graphics pipeline; capturing the variable content data message at a predetermined position within the pipeline; signaling when the variable content data message has reached the predetermined within the pipeline; and determining whether the captured variable content data

message corresponds to the inserted variable content data message. A signaling step may comprise generating an interrupt when the variable content data message reaches the bottom of the pipeline. The capturing step may comprise storing the variable content data message in a register, and the determining step may comprise reading the contents of that register.

In accordance with still another aspect provided by this invention, a command processor receives a variable content data message and passes the variable content data message through a pipeline to a pixel engine. The pixel engine includes a register that captures the variable content data message and signals when the variable content data message has reached the pixel engine.

A still additional aspect provided by this invention provides a token comprising a variable content data message being inserted into a stream of graphics commands. A graphics system provides a response to an inquiry as to whether the portions of the graphics stream before the token have been processed to allow synchronization of graphics system events.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other features and advantages provided by the invention will be better and more completely understood by referring to the following detailed description of presently preferred embodiments in conjunction with the drawings, of which:

FIG. **1** is an overall view of an example interactive computer graphics system;

FIG. **2** is a block diagram of the FIG. **1** example computer graphics system;

FIG. **3** is a block diagram of the example graphics and audio processor shown in FIG. **2**;

FIG. **4** is a block diagram of the example 3D graphics processor shown in FIG. **3**;

FIG. **5** is an example logical flow diagram of the FIG. **4** graphics and audio processor;

FIG. **6** is flowchart of example graphics pipeline synchronization using a synchronization token; and

FIGS. **7**A and **7**B show example alternative compatible implementations.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS OF THE INVENTION

FIG. **1** shows an example interactive 3D computer graphics system **50**. System **50** can be used to play interactive 3D video games with interesting stereo sound. It can also be used for a variety of other applications.

In this example, system **50** is capable of processing, interactively in real time, a digital representation or model of a three-dimensional world. System **50** can display some or all of the world from any arbitrary viewpoint. For example, system **50** can interactively change the viewpoint in response to real time inputs from handheld controllers **59***a*, **52***b* or other input devices. This allows the game player to see the world through the eyes of someone within or outside of the world. System **50** can be used for applications that do not require real time 3D interactive display (e.g., 2D display generation and/or non-interactive display), but the capability of displaying quality 3D images very quickly can be used to create very realistic and exciting game play or other graphical interactions.

To play a video game or other application using system **50**, the user first connects a main unit **54** to his or her color television set **56** or other display device by connecting a cable **58** between the two. Main unit **54** produces both video signals and audio signals for controlling color television set **56**. The video signals are what controls the images displayed on the television screen **59**, and the audio signals are played back as sound through television stereo loudspeakers **61**L, **61**R.

The user also needs to connect main unit **54** to a power source. This power source may be a conventional AC adapter (not shown) that plugs into a standard home electrical wall socket and converts the house current into a lower DC voltage signal suitable for powering the main unit **54**. Batteries could be used in other implementations.

The user may use hand controllers **52***a*, **52***b* to control main unit **54**. Controls **60** can be used, for example, to specify the direction (up or down, left or right, closer or further away) that a character displayed on television **56** should move within a 3D world. Controls **60** also provide input for other applications (e.g., menu selection, pointer/cursor control, etc.). Controllers **52** can take a variety of forms. In this example, controllers **52** shown each include controls **60** such as joysticks, push buttons and/or directional switches. Controllers **52** may be connected to main unit **54** by cables or wirelessly via electromagnetic (e.g., radio or infrared) waves.

To play an application such as a game, the user selects an appropriate storage medium **62** storing the video game or other application he or she wants to play, and inserts that storage medium into a slot **64** in main unit **54**. Storage medium **62** may, for example, be a specially encoded and/or encrypted optical and/or magnetic disk. The user may operate a power switch **66** to turn on main unit **54** and cause the main unit to begin running the video game or other application based on the software stored in the storage medium **62**. The user may operate controllers **52** to provide inputs to main unit **54**. For example, operating a control **60** may cause the game or other application to start. Moving other controls **60** can cause animated characters to move in different directions or change the user's point of view in a 3D world. Depending upon the particular software stored within the storage medium **62**, the various controls **60** on the controller **52** can perform different functions at different times.

Example Electronics of Overall System

FIG. **2** shows a block diagram of example components of system **50**. The primary components include:

- a main processor (CPU) **110**,
- a main memory **112**, and
- a graphics and audio processor **114**.

In this example, main processor **110** (e.g., an enhanced IBM Power PC 750) receives inputs from handheld controllers **108** (and/or other input devices) via graphics and audio processor **114**. Main processor **110** interactively responds to user inputs, and executes a video game or other program supplied, for example, by external storage media **62** via a mass storage access device **106** such as an optical disk drive. As one example, in the context of video game play, main processor **110** can perform collision detection and animation processing in addition to a variety of interactive and control functions.

In this example, main processor **110** generates 3D graphics and audio commands and sends them to graphics and audio processor **114**. The graphics and audio processor **114** processes these commands to generate interesting visual images on display **59** and interesting stereo sound on stereo loudspeakers **61**R, **61**L or other suitable sound-generating devices.

Example system **50** includes a video encoder **120** that receives image signals from graphics and audio processor **114** and converts the image signals into analog and/or digital video signals suitable for display on a standard display device such as a computer monitor or home color television set **56**. System **50** also includes an audio codec (compressor/decompressor) **122** that compresses and decompresses digitized audio signals and may also convert between digital and analog audio signaling formats as needed. Audio codec **122** can receive audio inputs via a buffer **124** and provide them to graphics and audio processor **114** for processing (e.g., mixing with other audio signals the processor generates and/or receives via a streaming audio output of mass storage access device **106**). Graphics and audio processor **114** in this example can store audio related information in an audio memory **126** that is available for audio tasks. Graphics and audio processor **114** provides the resulting audio output signals to audio codec **122** for decompression and conversion to analog signals (e.g., via buffer amplifiers **128**L, **128**R) so they can be reproduced by loudspeakers **61**L, **61**R.

Graphics and audio processor **114** has the ability to communicate with various additional devices that may be present within system **50**. For example, a parallel digital bus **130** may be used to communicate with mass storage access device **106** and/or other components. A serial peripheral bus **132** may communicate with a variety of peripheral or other devices including, for example:

- a programmable read-only memory and/or real time clock **134**,
- a modem **136** or other networking interface (which may in turn connect system **50** to a telecommunications network **138** such as the Internet or other digital network from/to which program instructions and/or data can be downloaded or uploaded), and
- flash memory **140**.

A further external serial bus **142** may be used to communicate with additional expansion memory **144** (e.g., a memory card) or other devices. Connectors may be used to connect various devices to busses **130**, **132**, **142**.

Example Graphics And Audio Processor

FIG. **3** is a block diagram of an example graphics and audio processor **114**. Graphics and audio processor **114** in one example may be a single-chip ASIC (application specific integrated circuit). In this example, graphics and audio processor **114** includes:

- a processor interface **150**,
- a memory interface/controller **152**,
- a 3D graphics processor **154**,
- an audio digital signal processor (DSP) **156**,
- an audio memory interface **158**,
- an audio interface and mixer **160**,
- a peripheral controller **162**, and
- a display controller **164**.

3D graphics processor **154** performs graphics processing tasks. Audio digital signal processor **156** performs audio processing tasks. Display controller **164** accesses image information from main memory **1 12** and provides it to video encoder **120** for display on display device **56**. Audio interface and mixer **160** interfaces with audio codec **122**, and can also mix audio from different sources (e.g., streaming audio from mass storage access device **106**, the output of audio DSP **156**, and external audio input received via audio codec **122**). Processor interface **150** provides a data and control interface between main processor **110** and graphics and audio processor **114**.

Memory interface **152** provides a data and control interface between graphics and audio processor **114** and memory **112**. In this example, main processor **110** accesses main memory **112** via processor interface **150** and memory interface **152** that are part of graphics and audio processor **114**. Peripheral controller **162** provides a data and control interface between graphics and audio processor **114** and the various peripherals mentioned above. Audio memory interface **158** provides an interface with audio memory **126**.

Example Graphics Pipeline

FIG. **4** shows a more detailed view of an example 3D graphics processor **154**. 3D graphics processor **154** includes, among other things, a command processor **200** and a 3D graphics pipeline **180**. Main processor **110** communicates streams of data (e.g., graphics command streams and display lists) to command processor **200**. Main processor **110** has a two-level cache **115** to minimize memory latency, and also has a write-gathering buffer **111** for uncached data streams targeted for the graphics and audio processor **114**. The write-gathering buffer **111** collects partial cache lines into full cache lines and sends the data out to the graphics and audio processor **114** one cache line at a time for maximum bus usage.

Command processor **200** receives display commands from main processor **110** and parses them—obtaining any additional data necessary to process them from shared memory **112**. The command processor **200** provides a stream of vertex commands to graphics pipeline **180** for 2D and/or 3D processing and rendering. Graphics pipeline **180** generates images based on these commands. The resulting image information may be transferred to main memory **112** for access by display controller/video interface unit **164**—which displays the frame buffer output of pipeline **180** on display **56**.

FIG. **5** is a logical flow diagram of graphics processor **154**. Main processor **110** may store graphics command streams **210**, display lists **212** and vertex arrays **214** in main memory **112**, and pass pointers to command processor **200** via bus interface **150**. The main processor **110** stores graphics commands in one or more graphics first-in-first-out (FIFO) buffers **210** it allocates in main memory **10**. The command processor **200** fetches:

- command streams from main memory **112** via an on-chip FIFO memory buffer **216** that receives and buffers the graphics commands for synchronization/flow control and load balancing,
- display lists **212** from main memory **112** via an on-chip call FIFO memory buffer **218**, and
- vertex attributes from the command stream and/or from vertex arrays **214** in main memory **112** via a vertex cache **220**.

Command processor **200** performs command processing operations **200***a* that convert attribute types to floating point format, and pass the resulting complete vertex polygon data to graphics pipeline **180** for rendering/rasterization. A programmable memory arbitration circuitry **130** (see FIG. **4**) arbitrates access to shared main memory **112** between graphics pipeline **180**, command processor **200** and display controller/video interface unit **164**.

FIG. **4** shows that graphics pipeline **180** may include:

- a transform unit **300**,
- a setup/rasterizer **400**,
- a texture unit **500**,
- a texture environment unit **600**, and
- a pixel engine **700**.

Transform unit **300** performs a variety of 2D and 3D transform and other operations **300***a* (see FIG. **5**). Transform

unit **300** may include one or more matrix memories **300***b* for storing matrices used in transformation processing **300***a*. Transform unit **300** transforms incoming geometry per vertex from object space to screen space; and transforms incoming texture coordinates and computes projective texture coordinates (**300***c*). Transform unit **300** may also perform polygon clipping/culling **300***d*. Lighting processing **300***e* also performed by transform unit **300***b* provides per vertex lighting computations for up to eight independent lights in one example embodiment. Transform unit **300** can also perform texture coordinate generation (**300***c*) for embossed type bump mapping effects, as well as polygon clipping/culling operations (**300***d*).

Setup/rasterizer **400** includes a setup unit which receives vertex data from transform unit **300** and sends triangle setup information to one or more rasterizer units (**400***b*) performing edge rasterization, texture coordinate rasterization and color rasterization.

Texture unit **500** (which may include an on-chip texture memory (TMEM) **502**) performs various tasks related to texturing including for example:

- retrieving textures **504** from main memory **112**,
- texture processing (**500***a*) including, for example, multi-texture handling, post-cache texture decompression, texture filtering, embossing, shadows and lighting through the use of projective textures, and BLIT with alpha transparency and depth,
- bump map processing for computing texture coordinate displacements for bump mapping, pseudo texture and texture tiling effects (**500***b*), and
- indirect texture processing (**500***c*).

Texture unit **500** outputs filtered texture values to the texture environment unit **600** for texture environment processing (**600***a*). Texture environment unit **600** blends polygon and texture color/alpha/depth, and can also perform texture fog processing (**600***b*) to achieve inverse range based fog effects. Texture environment unit **600** can provide multiple stages to perform a variety of other interesting environment-related functions based for example on color/alpha modulation, embossing, detail texturing, texture swapping, clamping, and depth blending.

Pixel engine **700** performs depth (z) compare (**700***a*) and pixel blending (**700***b*). In this example, pixel engine **700** stores data into an embedded (on-chip) frame buffer memory **702**. Graphics pipeline **180** may include one or more embedded DRAM memories **702** to store frame buffer and/or texture information locally. Z compares **700***a* can also be performed at an earlier stage in the graphics pipeline **180** depending on the rendering mode currently in effect (e.g., z compares can be performed earlier if alpha blending is not required). The pixel engine **700** includes a copy operation **700***c* that periodically writes on-chip frame buffer **702** to main memory **112** for access by display/video interface unit **164**. This copy operation **700***c* can also be used to copy embedded frame buffer **702** contents to textures in the main memory **112** for dynamic texture synthesis effects. Anti-aliasing and other filtering can be performed during the copy-out operation. The frame buffer output of graphics pipeline **180** (which is ultimately stored in main memory **112**) is read each frame by display/video interface unit **164**. Display controller/video interface **164** provides digital RGB pixel values for display on display **102**.

Graphics Pipeline Synchronization Mechanism

As shown in FIG. **4**, the rendering pipeline of system **50** consists of several asynchronous components. Among them are the main processor **110** generating graphics commands, the graphics and audio processor **114** consuming the commands and producing frame buffers, and the display controller/video interface **164** displaying the frame buffers. The present invention provides a mechanism to synchronize these components—allowing for various programming models with different levels of complexity.

In the example embodiment, main processor **110** should be coordinated with the graphics and audio processor **114**. For example, primitive data and texture data that the main processor **110** provides should remain available until the graphics and audio processor **114** has read it, after which the main processor can alter the data for the next frame or delete it as necessary. Also, the graphics and audio processor **114** should be coordinated with the display controller/video interface **164** such that the embedded frame buffer **702** is only copied to an inactive external frame buffer **113**, and the display controller/video interface **164** will switch to scanning out the new external frame buffer at the right time—freeing up the previously scanned-out external frame buffer for use by the next frame. Other applications for synchronization include other memory coherence tasks for portions of main memory **112** shared between the main processor **110** and the graphics and audio processor **114**.

One mechanism the example embodiment provides for synchronization is a so-called "draw done" command. In this particular example, the "draw done" command is a wrapper around two synchronization functions in the preferred embodiment: a "set draw done" and a "wait draw done." The "set draw done" command sends a draw-done token into a first in first out buffer between the main processor **110** and the graphics and audio processor **114** and flushes that buffer. The "wait draw done" command waits for the graphics pipeline **180** to flush and the token to appear at the bottom of the graphics pipeline. Instead of waiting for the token, one can also make use of a callback that happens as a result of a draw-done interrupt. This callback runs with interrupt disabled, and thus completes quickly. The function to set the callback routine may also return the previous callback function pointer.

In addition to the "draw done" synchronization mechanism described above, the preferred embodiment of system **50** also includes a "draw sync" command used to detect that the graphics pipeline **180** has completed processing of certain commands (e.g., completely rendered certain geometry). Using this "draw sync" mechanism, the programmer can send a variable content token, e.g., a 16-bit number of the main processor **110**'s choosing, down the graphics pipeline **180**. This token is stored in a token register **704** once it reaches a predetermined point in the graphics pipeline—in this particular example, the very bottom of the graphics pipeline within the pixel engine **700**. Main processor **110** can read token register **704** by sending an additional command to the graphics and audio processor **114**. When the token register value returned matches the token the main processor **110** has sent, the main processor knows that the particular geometry associated with the token has been completely rendered.

In more detail, the graphics and audio processor may include the following commands in its repertoire of synchronization commands:

- GXSetDrawSync (Token); and
- GXReadDrawSync (Token).

In these examples, the argument "Token" is a 16-bit unsigned integer value. In response to the GXSetDrawSync command, the graphics pipeline **180** hardware writes Token into token register **704** when this command reaches the bottom of the drawing pipeline. The register **704** can be read back (e.g., polled) to check the progress of drawing. In the

preferred embodiment, the GXDrawSync thus allows one to insert a number (16-bit token) into the graphics pipeline **180** and read the token value when it reaches the bottom of the graphics pipeline, without forcing the graphics pipeline to be flushed (and without creating a "bubble" of idle cycles within the graphics pipeline). The GXReadDrawSync command reads the token register **704** at the bottom of the graphics pipeline **180**, and returns the token value.

In a particular example implementation, an interrupt line **706** is provided from pixel engine **700** to processor interface **150**. This interrupt line **706** is associated with the token register **704** and associated function. Pixel engine **700** asserts this interrupt line **706** as active (e.g., high) when the token register **704** within pixel engine **700** has received and stored a token in response to the "GXSetDrawSync" command described above. This interrupt function can be enabled or disabled by main processor **10** by writing an interrupt enable value to a further interrupt control register (not shown) within pixel engine **700**. Main processor **110** can clear the interrupt once asserted by writing to the interrupt control register within the pixel engine **700**, and can poll the contents of token register **700** by sending the "ReadDrawSync" command described above.

In the preferred embodiment, an application running on main processor **110** can register a token interrupt callback asserting a "GXDrawSyncCallback" command. The callback's argument is the value of the most recently encountered token. Since it is possible to miss tokens (graphics processing does not stop while the callback is running), the application should be capable of deducing if any tokens have been missed (e.g., by using monotonically increasing values).

FIG. **6** shows an example flowchart using the token synchronization mechanism described above. The FIG. **6** flowchart might, for example, be performed by an application running on main processor **110**. In this particular example, the application inserts one or more graphics commands into the graphics pipeline **180** (block **800**), and generates a unique data message (block **802**) and inserts that unique data message into the graphics pipeline as a token using the SetDrawSync command described above (block **804**). In this particular example, the inserted token is a unique structured data object or message that comprises a non-reducible textual element in the data that is being parsed—for example, a variable name, a value, a number, a character or a word. The application may then perform other tasks while waiting for an interrupt from pixel engine **700** (block **806**). Once the interrupt is received, the application may read pixel engine token register **704** using the GetDrawSync command discussed (block **808**). When the application retrieves the contents of token register **704** it may compare that value with a particular value it sent as a token to determine whether the value matches (decision block **810**). If the comparison is favorable, then the application may perform a task (block **812**) requiring synchronization with the graphics pipeline **180**—since the application "knows" that the graphics pipeline **180** has finished processing command(s) inserted prior to the token by block **800**.

The following is an example usage:

```
void GXSetDrawSync(u16 token);
u16 GXReadDrawSync( );
typedef void (*GXDrawSyncCallback)(u16 token);
GXDrawSyncCallback GXSetDrawSyncCallback
(GXDrawSyncCallback cb);
```

The synchronization token described above permits applications running on main processor **110** to define any number of different synchronization events, and distinguish between those synchronization events based on token value. In the preferred embodiment, the graphics pipeline **180** does not modify the token value so that the main processor **110** can easily recognize it—but in other embodiments, the graphics pipeline **180** could perform a predetermined function on the token value to change its value without destroying the ability of the main processor **110** to correlate tokens it inserts into the graphics pipeline **180** with token values received at the pixel engine **700**. In the preferred embodiment, the token register **704** is disposed at the very bottom of the graphics pipeline **180**, but it could be disposed at other places—or multiple token registers and associated interrupt lines could be provided if desired to monitor geometry completion states other than final completion. One useful application of this synchronization mechanism is when main processor **110** writes to memory separate from the graphics pipeline **180** (e.g., a main memory **112** that is shared between the main processor **110** and the graphics pipeline **180**) and wants to maintain memory coherence.

Other Example Compatible Implementations

Certain of the above-described system components **50** could be implemented as other than the home video game console configuration described above. For example, one could run graphics application or other software written for system **50** on a platform with a different configuration that emulates system **50** or is otherwise compatible with it. If the other platform can successfully emulate, simulate and/or provide some or all of the hardware and software resources of system **50**, then the other platform will be able to successfully execute the software.

As one example, an emulator may provide a hardware and/or software configuration (platform) that is different from the hardware and/or software configuration (platform) of system **50**. The emulator system might include software and/or hardware components that emulate or simulate some or all of hardware and/or software components of the system for which the application software was written. For example, the emulator system could comprise a general purpose digital computer such as a personal computer, which executes a software emulator program that simulates the hardware and/or firmware of system **50**.

Some general purpose digital computers (e.g., IBM or MacIntosh personal computers and compatibles) are now equipped with 3D graphics cards that provide 3D graphics pipelines compliant with DirectX or other standard 3D graphics command APIs. They may also be equipped with stereophonic sound cards that provide high quality stereophonic sound based on a standard set of sound commands. Such multimedia-hardware-equipped personal computers running emulator software may have sufficient performance to approximate the graphics and sound performance of system **50**. Emulator software controls the hardware resources on the personal computer platform to simulate the processing, 3D graphics, sound, peripheral and other capabilities of the home video game console platform for which the game programmer wrote the game software.

FIG. 7A illustrates an example overall emulation process using a host platform **1201**, an emulator component **1303**, and a game software executable binary image provided on a

storage medium **62**. Host **1201** may be a general or special purpose digital computing device such as, for example, a personal computer, a video game console, or any other platform with sufficient computing power. Emulator **1303** may be software and/or hardware that runs on host platform **1201**, and provides a real-time conversion of commands, data and other information from storage medium **62** into a form that can be processed by host **1201**. For example, emulator **1303** fetches "source" binary-image program instructions intended for execution by system **50** from storage medium **62** and converts these program instructions to a target format that can be executed or otherwise processed by host **1201**.

As one example, in the case where the software is written for execution on a platform using an IBM PowerPC or other specific processor and the host **1201** is a personal computer using a different (e.g., Intel) processor, emulator **1303** fetches one or a sequence of binary-image program instructions from storage medium **1305** and converts these program instructions to one or more equivalent Intel binary-image program instructions. The emulator **1303** also fetches and/or generates graphics commands and audio commands intended for processing by the graphics and audio processor **114**, and converts these commands into a format or formats that can be processed by hardware and/or software graphics and audio processing resources available on host **1201**. As one example, emulator **1303** may convert these commands into commands that can be processed by specific graphics and/or or sound hardware of the host **1201** (e.g., using standard DirectX, OpenGL and/or sound APIs).

An emulator **1303** used to provide some or all of the features of the video game system described above may also be provided with a graphic user interface (GUI) that simplifies or automates the selection of various options and screen modes for games run using the emulator. In one example, such an emulator **1303** may further include enhanced functionality as compared with the host platform for which the software was originally intended.

FIG. **7**B illustrates an emulation host system **1201** suitable for use with emulator **1303**. System **1201** includes a processing unit **1203** and a system memory **1205**. A system bus **1207** couples various system components including system memory **1205** to processing unit **1203**. System bus **1207** may be any of several types of bus structures including a memory bus or memory controller a peripheral bus, and a local bus using any of a variety of bus architectures. System memory **1207** includes read only memory (ROM) **1252** and random access memory (RAM) **1254**. A basic input/output system (BIOS) **1256**, containing the basic routines that help to transfer information between elements within personal computer system **1201**, such as during start-up, is stored in the ROM **1252**. System **1201** further includes various drives and associated computer-readable media. A hard disk drive **1209** reads from and writes to a (typically fixed) magnetic hard disk **1211**. An additional (possible optional) magnetic disk drive **1213** reads from and writes to a removable "floppy" or other magnetic disk **1215**. An optical disk drive **1217** reads from and, in some configurations, writes to a removable optical disk **1219** such as a CD ROM or other optical media. Hard disk drive **1209** and optical disk drive **1217** are connected to system bus **1207** by a hard disk drive interface **1221** and an optical drive interface **1225**, respectively. The drives and their associated computer-readable media provide nonvolatile storage of computer-readable instructions, data structures, program modules, game programs and other data for personal computer system **1201**. In other configurations, other types of computer-readable media that can store data that is accessible by a computer (e.g., magnetic cassettes, flash memory cards, digital video disks, Bernoulli cartridges, random access memories (RAMs), read only memories (ROMs) and the like) may also be used.

A number of program modules including emulator **1303** may be stored on the hard disk **1211**, removable magnetic disk **1215**, optical disk **1219** and/or the ROM **1252** and/or the RAM **1254** of system memory **1205**. Such program modules may include an operating system providing graphics and sound APIs, one or more application programs, other program modules, program data and game data. A user may enter commands and information into personal computer system **1201** through input devices such as a keyboard **1227**, pointing device **1229**, microphones, joysticks, game controllers, satellite dishes, scanners, or the like. These and other input devices can be connected to processing unit **1203** through a serial port interface **1231** that is coupled to system bus **1207**, but may be connected by other interfaces, such as a parallel port, game port Fire wire bus or a universal serial bus (USB). A monitor **1233** or other type of display device is also connected to system bus **1207** via an interface, such as a video adapter **1235**.

System **1201** may also include a modem **1154** or other network interface means for establishing communications over a network **1152** such as the Internet. Modem **1154**, which may be internal or external, is connected to system bus **123** via serial port interface **1231**. A network interface **1156** may also be provided for allowing system **1201** to communicate with a remote computing device **1150** (e.g., another system **1201**) via a local area network **1158** (or such communication may be via wide area network **1152** or other communications path such as dial-up or other communications means). System **1201** will typically include other peripheral output devices, such as printers and other standard peripheral devices.

In one example, video adapter **1235** may include a 3D graphics pipeline chip set providing fast 3D graphics rendering in response to 3D graphics commands issued based on a standard 3D graphics application programmer interface such as Microsoft's DirectX 7.0 or other version. A set of stereo loudspeakers **1237** is also connected to system bus **1207** via a sound generating interface such as a conventional "sound card" providing hardware and embedded software support for generating high quality stereophonic sound based on sound commands provided by bus **1207**. These hardware capabilities allow system **1201** to provide sufficient graphics and sound speed performance to play software stored in storage medium **62**.

All documents referenced above are hereby incorporated by reference.

While the invention has been described in connection with what is presently considered to be the most practical and preferred embodiment, it is to be understood that the invention is not to be limited to the disclosed embodiment, but on the contrary, is intended to cover various modifications and equivalent arrangements included within the scope of the appended claims.

We claim:

1. A method of synchronizing at least one process external to a graphics pipeline with the graphics pipeline comprising:

sending a programmable content synchronization token down the graphics pipeline;

detecting when the synchronization token has reached a predetermined point in the pipeline; and

signaling the external process when the synchronization token has been detected to reach said predetermined point in the pipeline.

2. The method of claim 1 wherein the synchronization token comprises a variable content data message the graphics pipeline does not modify.

3. The method of claim 1 wherein the detecting step comprises comparing a value returned by a token register with the value of the sent synchronization token.

4. The method of claim 1 further including specifying, with an application program, a variable synchronization token value to send down the graphics pipeline.

5. The method of claim 1 wherein the synchronization token comprises a 16-bit variable value.

6. The method of claim 1 wherein the detecting step includes polling a synchronization token register at the end of the pipeline in response to an interrupt.

7. A method of synchronizing at least one process external to a graphics pipeline with the graphics pipeline, said graphics pipeline being of the type including a command processor, a transformation unit, a lighting unit, a texture coordinate generator, a texture mapper, a rasterizer, a blender, a pixel engine and a frame buffer, the method comprising:

inserting a variable content synchronization message into the graphics pipeline;

capturing the variable content synchronization message at a predetermined position within the pipeline;

signaling the external process when the variable content synchronization message has reached the predetermined position within the pipeline; and

testing whether the captured variable content synchronization message corresponds to the inserted variable content synchronization message.

8. The method of claim 7 wherein the signaling step comprises generating an interrupt when the variable content synchronization message reaches the bottom of the pipeline.

9. The method of claim 7 wherein the capturing step comprises storing the variable content synchronization message in a register, and the determining step includes reading the contents of the register.

10. The method of claim 7 wherein the pixel engine performs the signaling step.

11. The method of claim 7 wherein the graphics pipeline does not modify the variable content synchronization message.

12. A graphics pipeline including:

a command processor,

a transformation unit,

a lighting unit,

a texture coordinate generator,

a texture mapper,

a rasterizer,

a blender,

a pixel engine, and

a frame buffer,

wherein the command processor receives a variable content synchronization message and passes the variable content synchronization message through the graphics pipeline to the pixel engine, the pixel engine including a register that captures the variable content synchronization message and signals at least one process external to the graphics pipeline when the variable content synchronization message has reached the pixel engine.

13. The graphics pipeline of claim 12 wherein the graphics pipeline does not alter the variable content synchronization message.

14. A graphics system of the type that receives a stream of graphics commands and generates an image based on the graphics command stream, the graphics system being adapted to receive, within the stream of graphics commands, a synchronization token comprising a variable content synchronization message, the graphics system providing a response to an inquiry as to whether portions of the graphics stream earlier in a graphics command sequence with respect to the synchronization token have been processed to allow synchronization of graphics system events with at least one process external to the graphics command stream processing.

15. The graphics system as in claim 14 wherein the graphics system includes an application specific integrated circuit.

16. The graphics system as in claim 14 wherein the graphics system includes a 3D graphics pipeline.

17. A method of synchronizing a process external to a 3D graphics pipeline with the 3D graphics pipeline, the 3D graphics pipeline being of the type including command processing, transformation, lighting, texture coordinate generation, texture mapping, rasterizing, and blending, an improvement comprising:

inserting a variable content synchronizing token into the graphics pipeline; and

signaling the external process upon the token reaching a predetermined point in the graphics pipeline.

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