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Leather

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(54) **3D GRAPHICS RENDERING SYSTEM FOR PERFORMING Z VALUE CLAMPING IN NEAR-Z RANGE TO MAXIMIZE SCENE RESOLUTION OF VISUALLY IMPORTANT Z COMPONENTS**

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(58) **Field of Search** 345/419, 421, 345/422, 427, 428, 506, 620, 627

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(57) **ABSTRACT**

A graphics system including a custom graphics and audio processor produces exciting 2D and 3D graphics and surround sound. The system includes a graphics and audio processor including a 3D graphics pipeline and an audio digital signal processor. The graphics pipeline performs Z-buffering and optionally provides memory efficient full scene anti-aliasing (FSAA). When the anti-aliasing rendering mode is selected, Z value bit compression is performed to more efficiently make use of the available Z buffer memory. A Z-clamping arrangement is used to improve the precision of visually important Z components by clamping Z values to zero of pixels that fall within a predetermined Z-axis range near the Z=0 eye/camera (viewport) plane. This allows a Z-clipping plane to be used very close to the eye/camera plane—to avoid undesirable visual artifacts produced when objects rendered near to the eye/camera plane are clipped—while preserving Z value precision for the remaining depth of the scene. In an example implementation, a Z value compression circuit provided in the graphics pipeline is enhanced to effectuate Z-clamping within the predetermined range of Z values. The enhanced circuitry includes an adder for left-shifting an input Z value one or more bits prior to compression and gates for masking out the most significant non-zero shifted bits to zero.

7 Claims, 10 Drawing Sheets

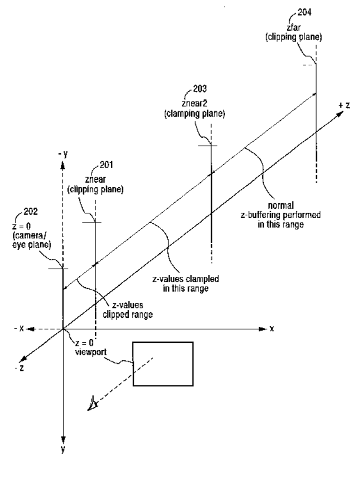

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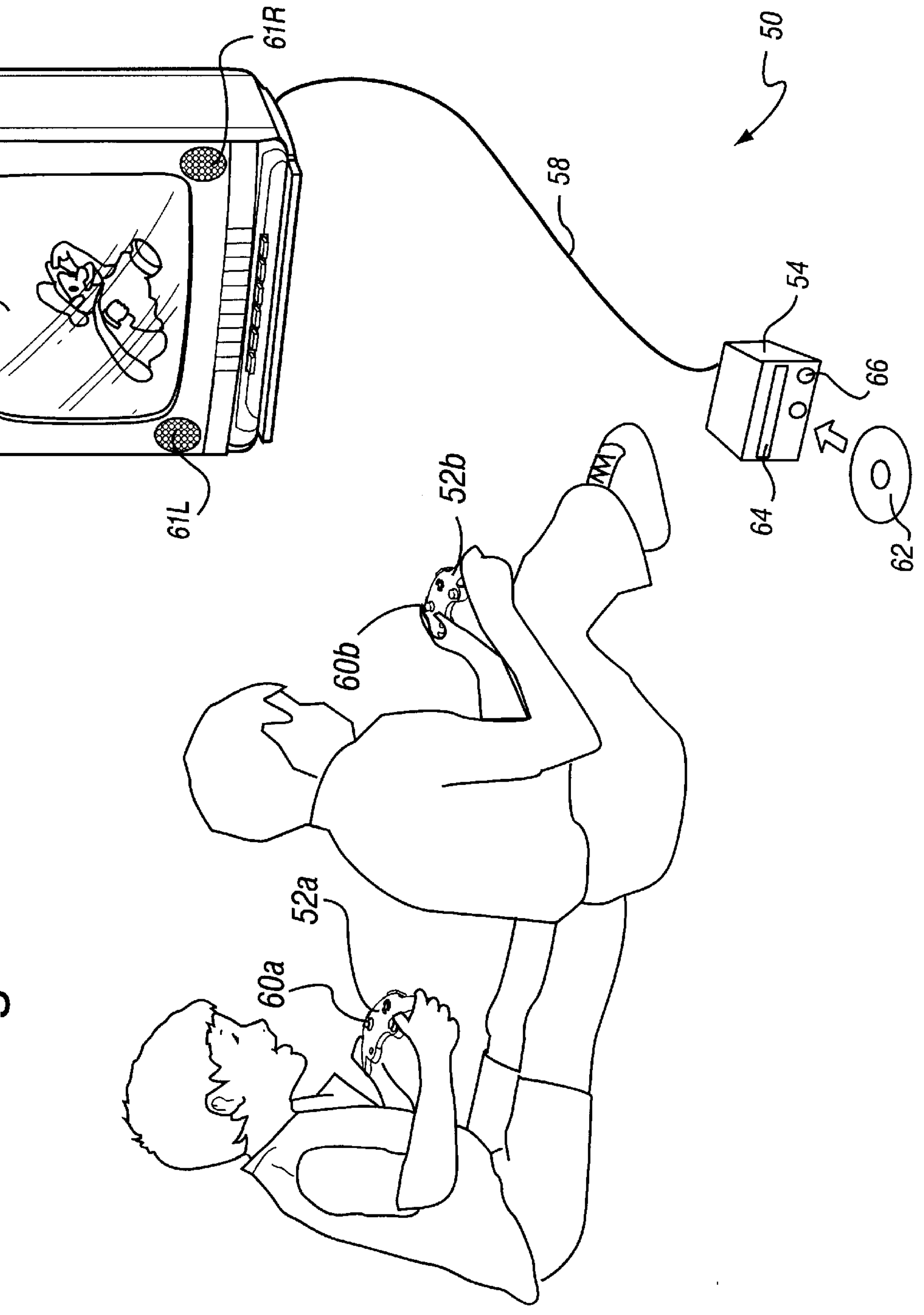
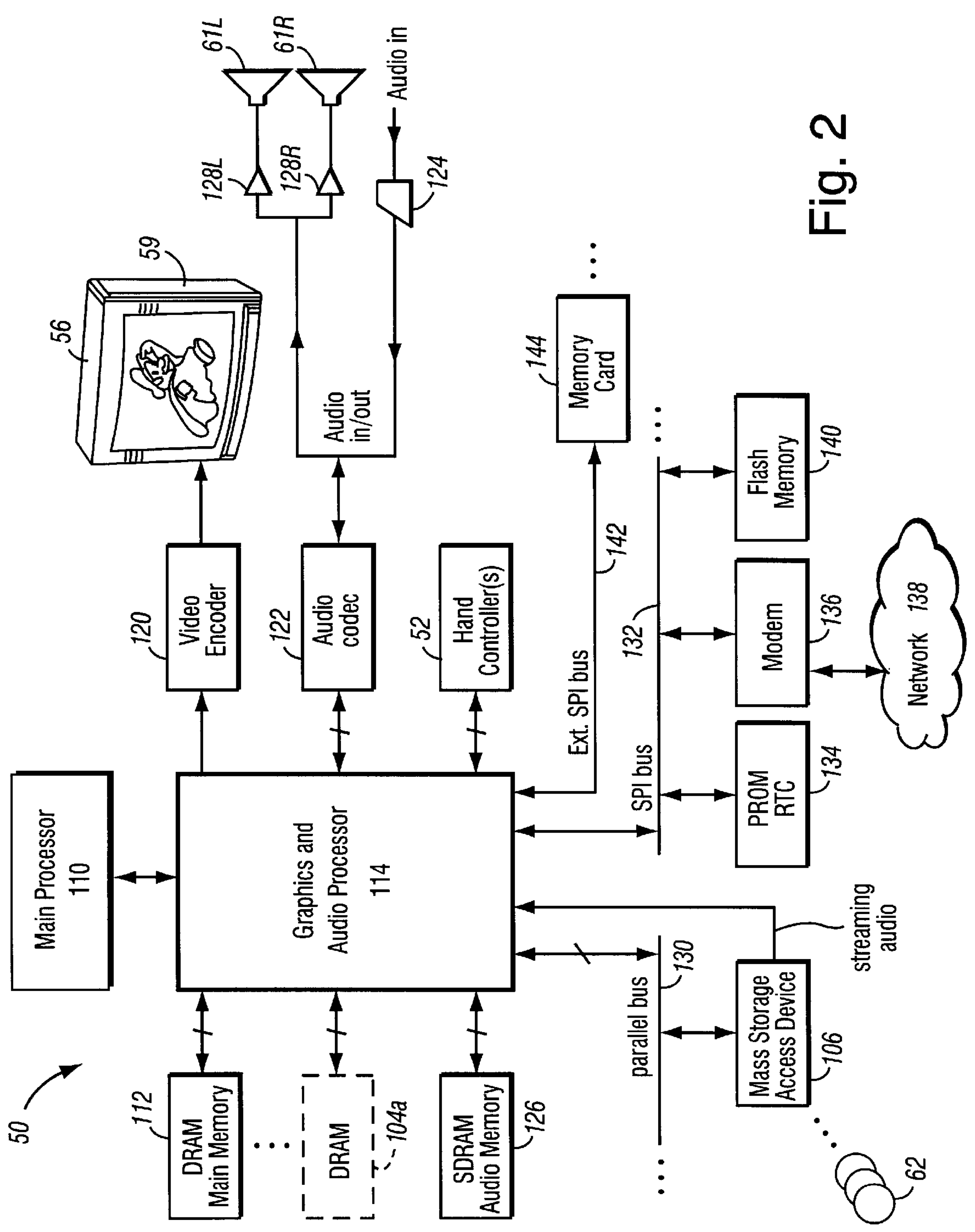
Fig. 1

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Graphics and Audio Processor 114
DRAM Main Memory 112
DRAM 104a
SDRAM Audio Memory 126
Video Encoder 120
Audio codec 122
Hand Controller(s) 52
56
59
Audio in/out
128L
128R
61L
61R
124
Audio in
Ext. SPI bus
142
Memory Card 144
SPI bus
132
PROM RTC 134
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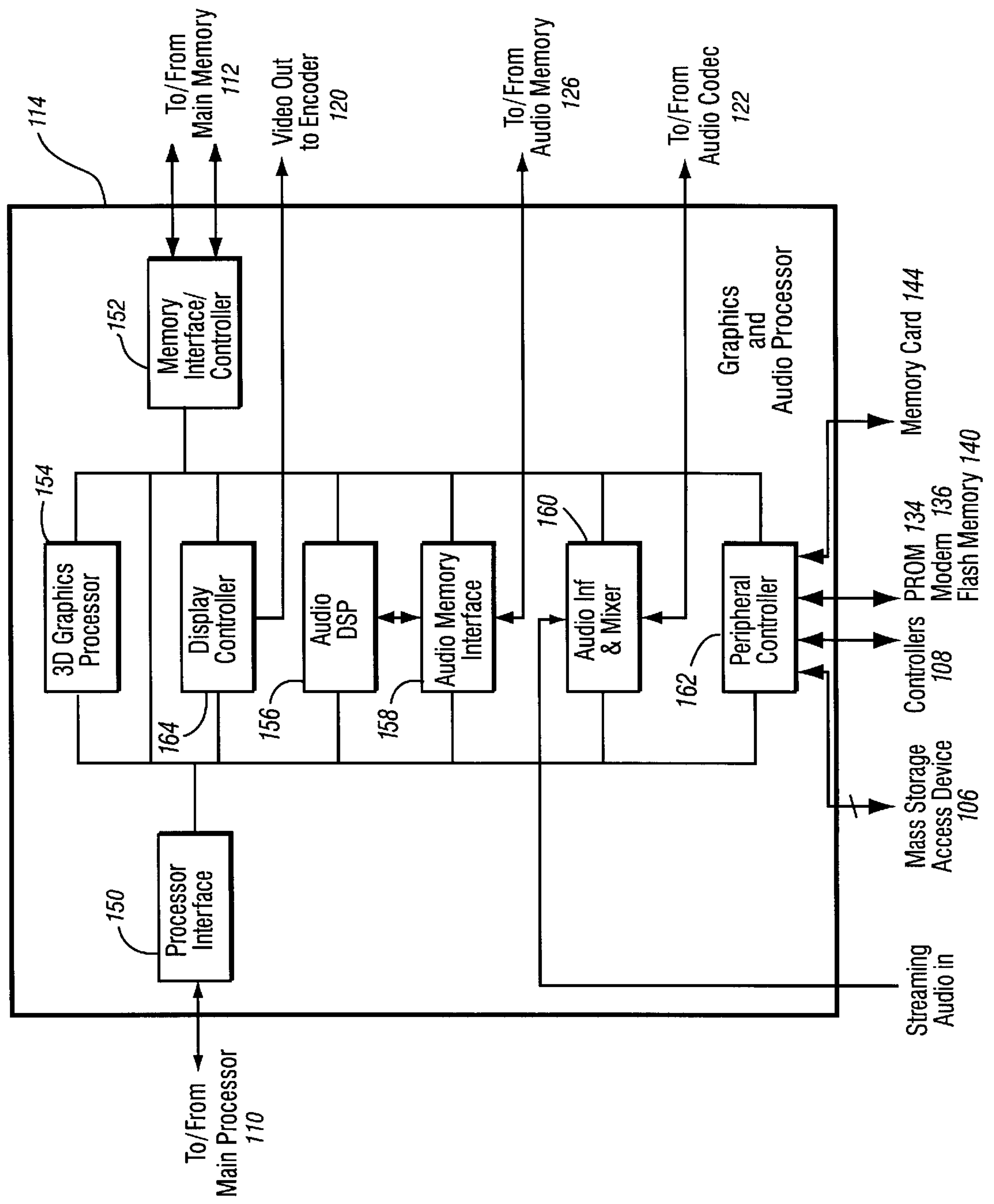
Flash Memory 140
Network 138
parallel bus
130
Mass Storage Access Device 106
streaming audio
62

Fig. 2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To/From Main Memory 112
Video Out to Encoder 120
To/From Audio Memory 126
To/From Audio Codec 122
152
Memory Interface/ Controller
Graphics and Audio Processor
154
3D Graphics Processor
Display Controller
164
Audio DSP
156
Audio Memory Interface
158
160
Audio Inf & Mixer
Peripheral Controller
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Streaming Audio in
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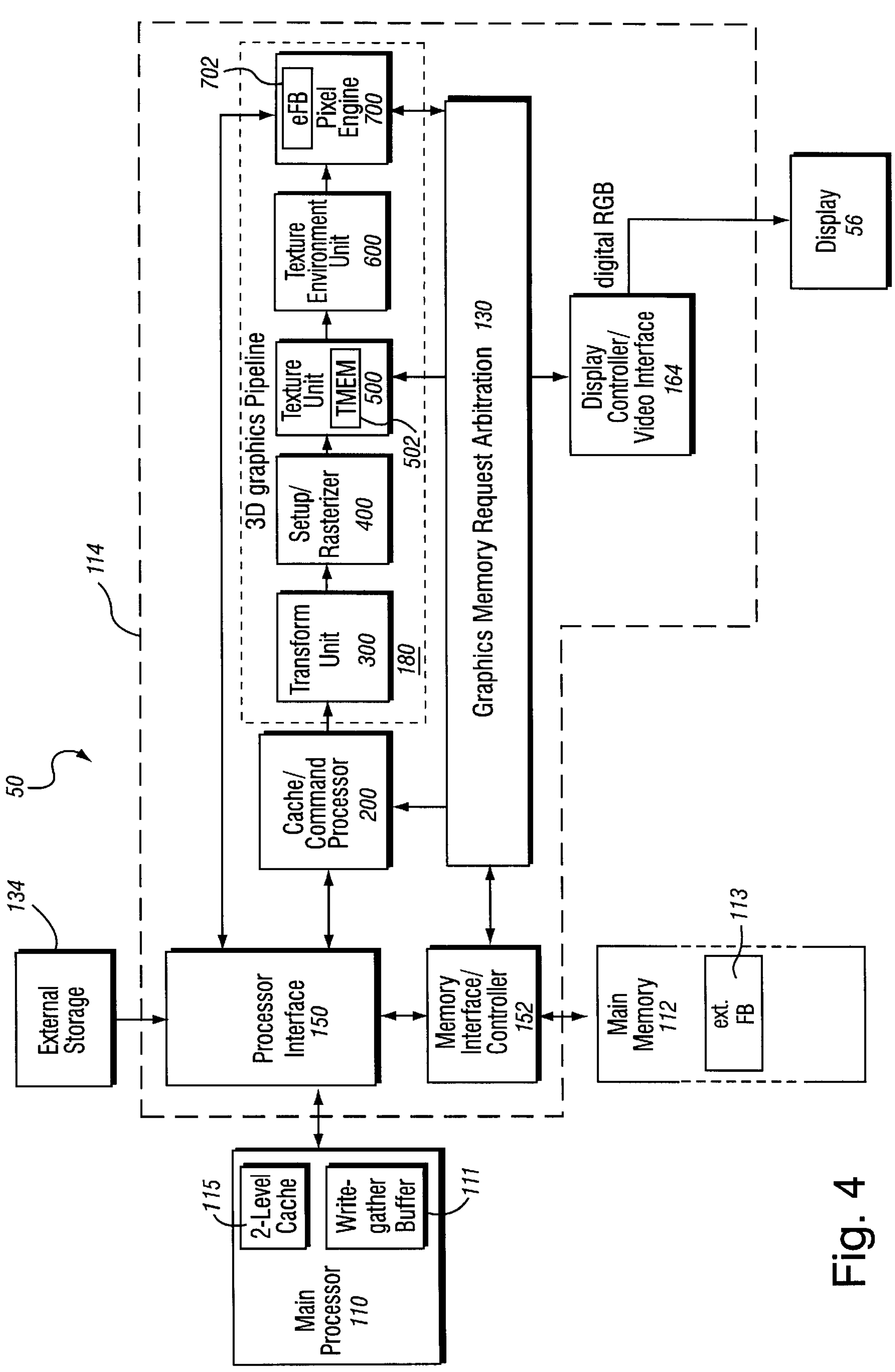
Fig. 3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114
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2-Level Cache
115
Write-gather Buffer
111
Cache/ Command Processor 200
Transform Unit 300
180
Setup/ Rasterizer 400
Texture Unit
TMEM
500
502
Texture Environment Unit 600
eFB
702
Pixel Engine 700
3D graphics Pipeline
Graphics Memory Request Arbitration 130
Display Controller/ Video Interface 164
digital RGB
Display 56

Fig. 4

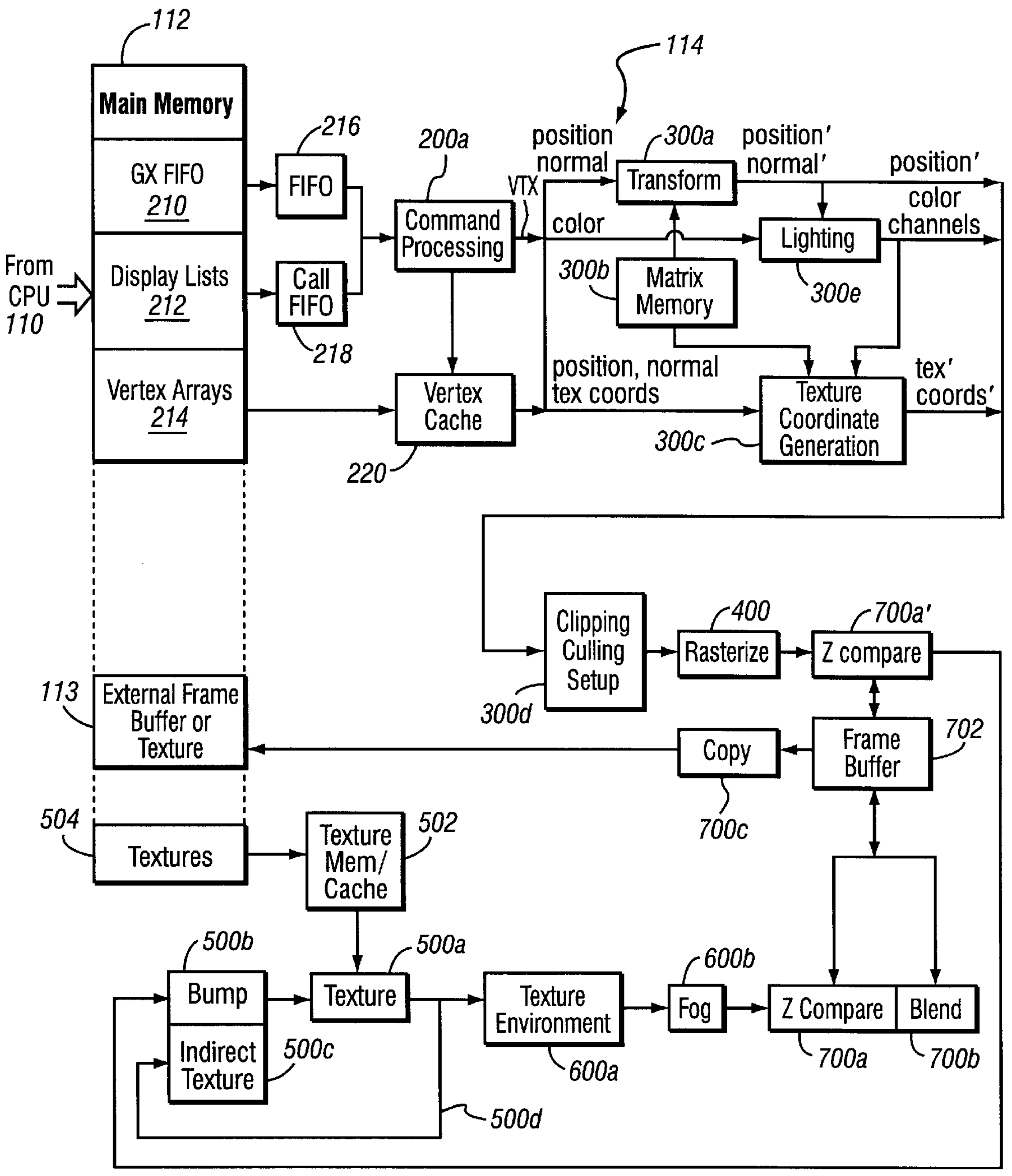

Fig. 5 EXAMPLE GRAPHICS PROCESSOR FLOW

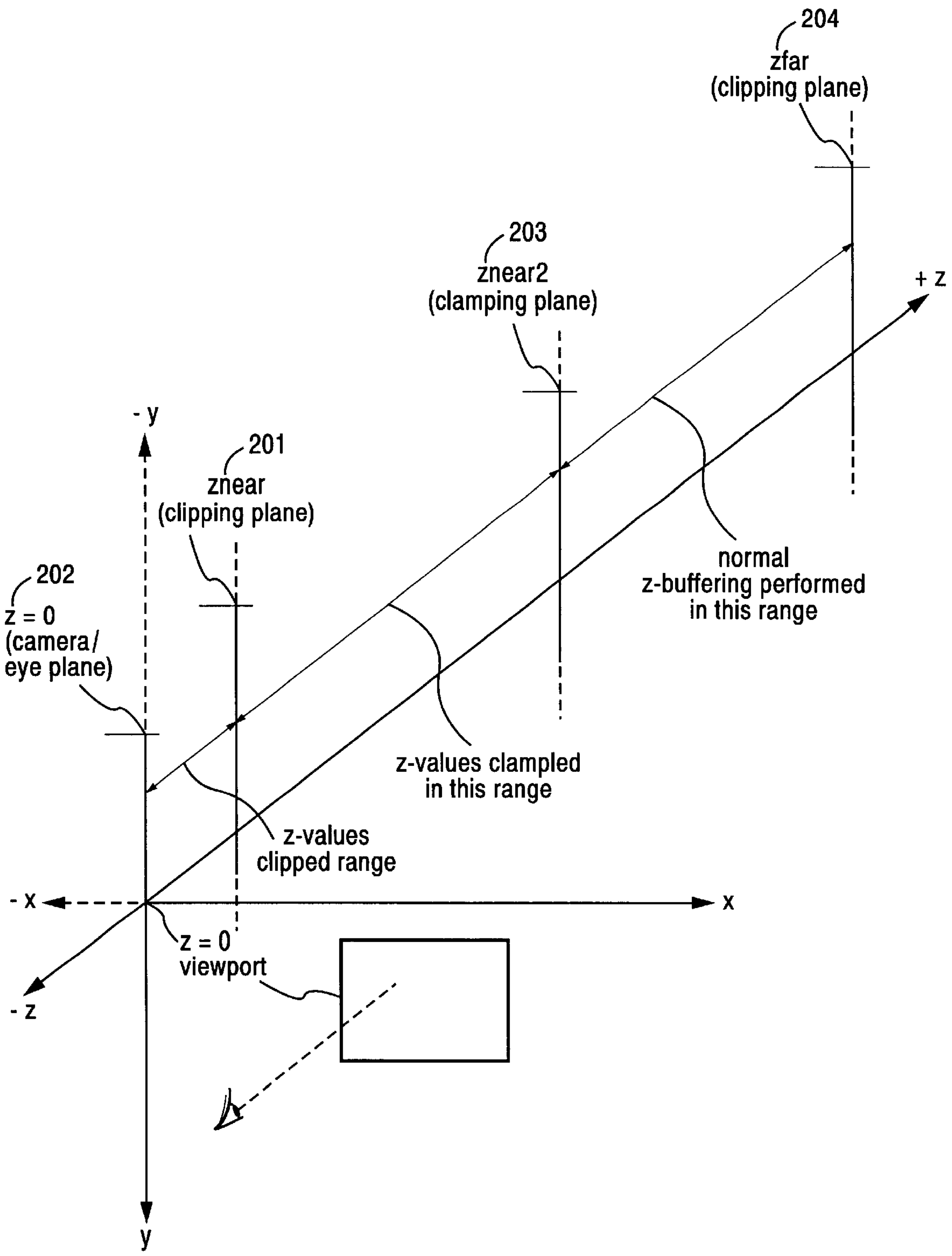
204
zfar
(clipping plane)
203
znear2
(clamping plane)
+ z
- y
201
znear
(clipping plane)
202
z = 0
(camera/
eye plane)
normal
z-buffering performed
in this range
z-values clampled
in this range
z-values
clipped range
- x
x
z = 0
viewport
- z
y

Fig. 6

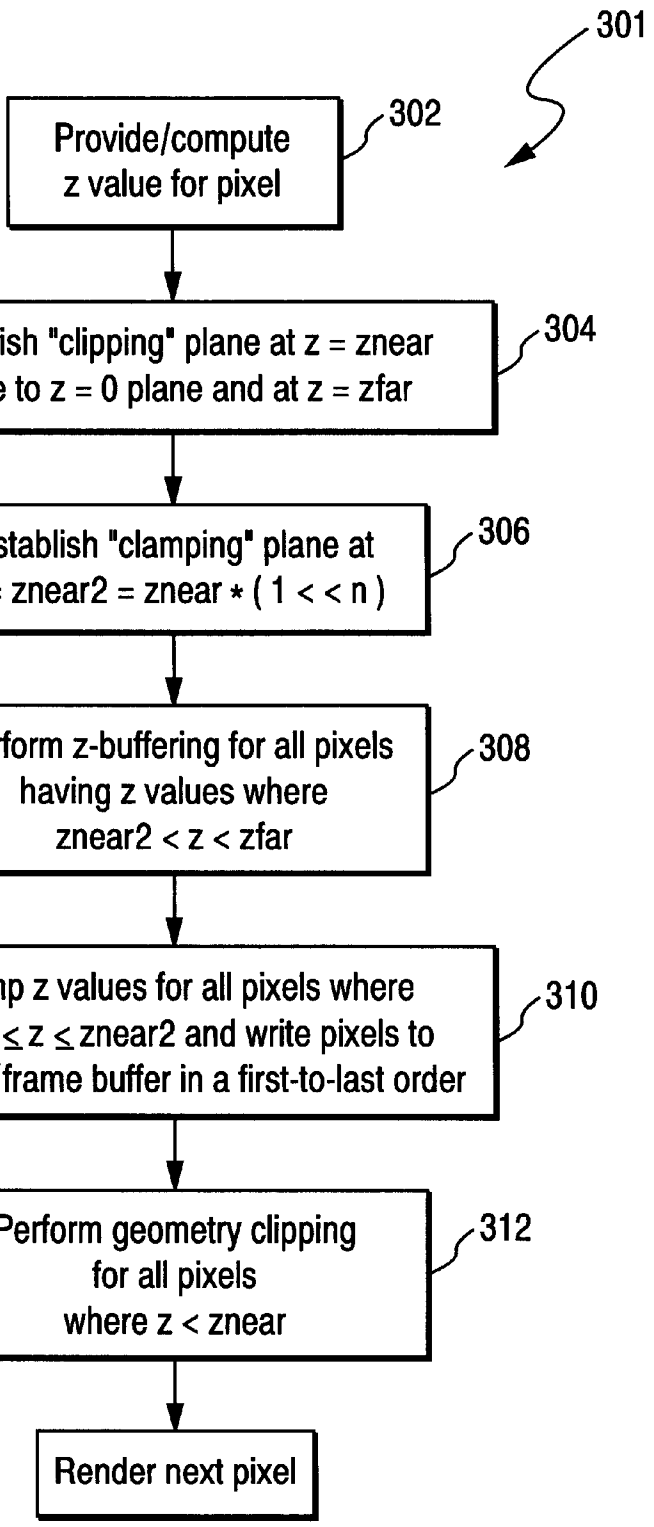
301
Provide/compute z value for pixel
302
Establish "clipping" plane at z = znear close to z = 0 plane and at z = zfar
304
Establish "clamping" plane at z = znear2 = znear * (1 < < n)
306
Perform z-buffering for all pixels having z values where znear2 < z < zfar
308
Clamp z values for all pixels where znear ≤ z ≤ znear2 and write pixels to z-buffer/frame buffer in a first-to-last order
310
Perform geometry clipping for all pixels where z < znear
312
Render next pixel

Fig. 7

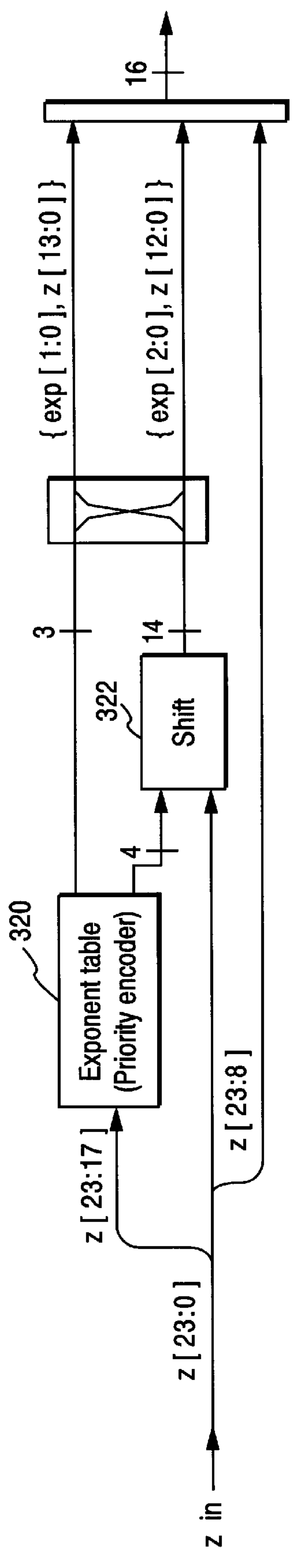
z in
z [23:0]
z [23:17]
z [23:8]
320
Exponent table (Priority encoder)
4
322
Shift
3
14
{ exp [1:0], z [13:0] }
{ exp [2:0], z [12:0] }
16

Fig. 8A

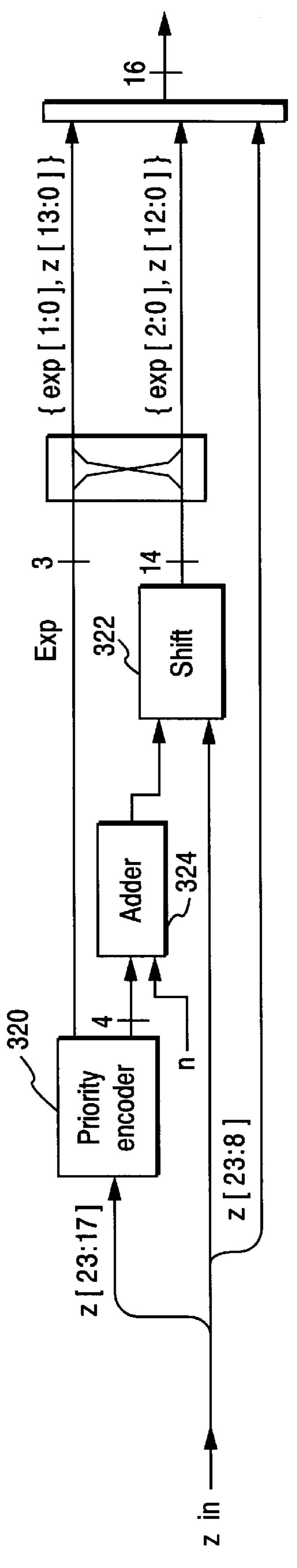
z in
z [23:17]
z [23:8]
320
Priority encoder
4
n
Adder
324
322
Shift
Exp
3
14
{ exp [1:0], z [13:0] }
{ exp [2:0], z [12:0] }
16

Fig. 8B

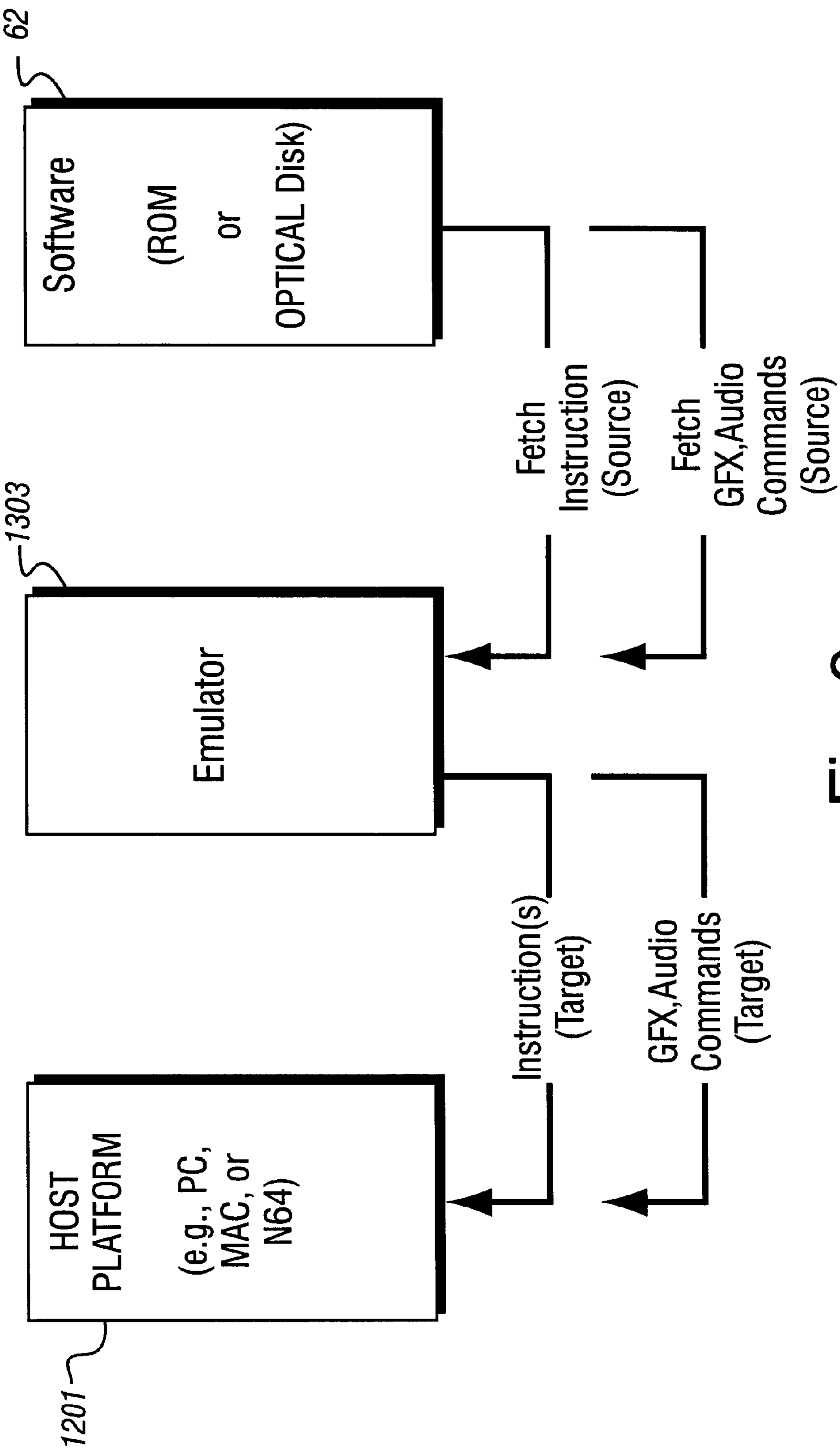
62
Software
(ROM
or
OPTICAL Disk)
Fetch
Instruction
(Source)
Fetch
GFX,Audio
Commands
(Source)
1303
Emulator
Instruction(s)
(Target)
GFX,Audio
Commands
(Target)
HOST
PLATFORM
(e.g., PC,
MAC, or
N64)
1201

Fig. 9

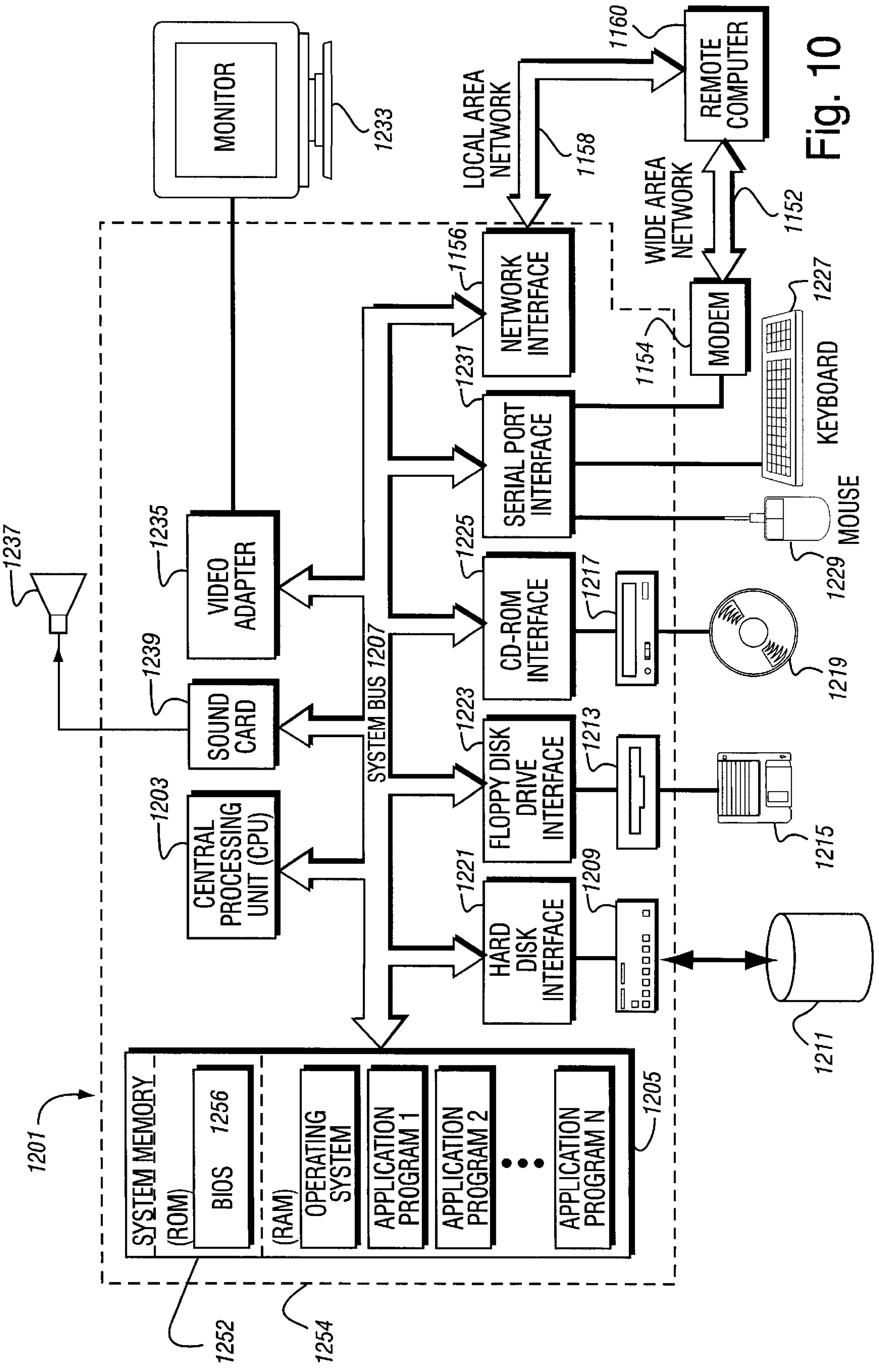
MONITOR
1233
LOCAL AREA NETWORK
1158
1160
REMOTE COMPUTER
WIDE AREA NETWORK
1152
1156
NETWORK INTERFACE
1154
MODEM
1227
KEYBOARD
1231
SERIAL PORT INTERFACE
MOUSE
1229
1235
VIDEO ADAPTER
1237
1239
SOUND CARD
1225
CD-ROM INTERFACE
1217
1219
SYSTEM BUS 1207
1203
CENTRAL PROCESSING UNIT (CPU)
1223
FLOPPY DISK DRIVE INTERFACE
1213
1215
1221
HARD DISK INTERFACE
1209
1211
1201
SYSTEM MEMORY
(ROM)
BIOS 1256
(RAM)
OPERATING SYSTEM
APPLICATION PROGRAM 1
APPLICATION PROGRAM 2
APPLICATION PROGRAM N
1205
1252
1254

Fig. 10

3D GRAPHICS RENDERING SYSTEM FOR PERFORMING Z VALUE CLAMPING IN NEAR-Z RANGE TO MAXIMIZE SCENE RESOLUTION OF VISUALLY IMPORTANT Z COMPONENTS

CROSS-REFERENCES TO RELATED APPLICATIONS

This application is related to the following commonly assigned applications identified below, which focus on various aspects of the graphics system described herein. Each of the following applications are incorporated herein by reference:

provisional application No. 60/161,915, filed Oct. 28, 1999 and its corresponding utility application Ser. No. 09/465,754, filed Dec. 17, 1999, both entitled "Vertex Cache For 3D Computer Graphics";

provisional application No. 60/226,912, filed Aug. 23, 2000 and its corresponding utility application Ser. No. 09/726,215, filed Nov. 28, 2000, both entitled "Method and Apparatus for Buffering Graphics Data in a Graphics System";

provisional application No. 60/226,889, filed Aug. 23, 2000 and its corresponding utility application Ser. No. 09/722,419, filed Nov. 28, 2000, both entitled "Graphics Pipeline Token Synchronization";

provisional application No. 60/226,891, filed Aug. 23, 2000 and its corresponding utility application Ser. No. 09/722,382, filed Nov. 28, 2000, both entitled "Method And Apparatus For Direct and Indirect Texture Processing In A Graphics System";

provisional application No. 60/226,888, filed Aug. 23, 2000 and its corresponding utility application Ser. No. 09/722,367, filed Nov. 28, 2000, both entitled "Recirculating Shade Tree Blender For A Graphics System";

provisional application No. 60/226,893, filed Aug. 23, 2000 and its corresponding utility application Ser. No. 09/722,381 filed Nov. 28, 2000, both entitled "Method And Apparatus For Environment-Mapped Bump-Mapping In A Graphics System";

provisional application No. 60/227,007, filed Aug. 23, 2000 and its corresponding utility application Ser. No. 09/726,216, filed Nov. 28, 2000, both entitled "Achromatic Lighting in a Graphics System and Method";

provisional application No. 60/226,900, filed Aug. 23, 2000 and its corresponding utility application Ser. No. 09/726,226, filed Nov. 28, 2000, both entitled "Method And Apparatus For Anti-Aliasing In A Graphics System";

provisional application No. 60/226,910, filed Aug. 23, 2000 and its corresponding utility application Ser. No. 09/722,380, filed Nov. 28, 2000, both entitled "Graphics System With Embedded Frame Buffer Having Reconfigurable Pixel Formats";

utility application Ser. No. 09/585,329, filed Jun. 2, 2000, entitled "Variable Bit Field Color Encoding";

provisional application No. 60/226,890, filed Aug. 23, 2000 and its corresponding utility application Ser. No. 09/726,227, filed Nov. 28, 2000, both entitled "Method And Apparatus For Dynamically Reconfiguring The Order Of Hidden Surface Processing Based On Rendering Mode";

provisional application No. 60/226,915, filed Aug. 23, 2000 and its corresponding utility application Ser. No. 09/726,212 filed Nov. 28, 2000, both entitled "Method And Apparatus For Providing Non-Photorealistic Cartoon Outlining Within A Graphics System";

provisional application No. 60/227,032, filed Aug. 23, 2000 and its corresponding utility application Ser. No. 09/726,225, filed Nov. 28, 2000, both entitled "Method And Apparatus For Providing Improved Fog Effects In A Graphics System";

provisional application No. 60/226,885, filed Aug. 23, 2000 and its corresponding utility application Ser. No. 09/722,664, filed Nov. 28, 2000, both entitled "Controller Interface For A Graphics System";

provisional application No. 60/227,033, filed Aug. 23, 2000 and its corresponding utility application Ser. No. 09/726,221, filed Nov. 28, 2000, both entitled "Method And Apparatus For Texture Tiling In A Graphics System";

provisional application No. 60/226,899, filed Aug. 23, 2000 and its corresponding utility application Ser. No. 09/722,667, filed Nov. 28, 2000, both entitled "Method And Apparatus For Pre-Caching Data In Audio Memory";

provisional application No. 60/226,913, filed Aug. 23, 2000 and its corresponding utility application Ser. No. 09/722,378, filed Nov. 28, 2000, both entitled "Z-Texturing";

provisional application No. 60/227,031, filed Aug. 23, 2000 entitled "Application Program Interface for a Graphics System",

provisional application No. 60/227,030, filed Aug. 23, 2000 and its corresponding utility application Ser. No. 09/722,663, filed Nov. 28, 2000, both entitled "Graphics System With Copy Out, Conversions Between Embedded Frame Buffer And Main Memory";

provisional application No. 60/226,886, filed Aug. 23, 2000 and its corresponding utility application Ser. No. 09/722,665, filed Nov. 28, 2000, both entitled "Method and Apparatus for Accessing Shared Resources";

provisional application No. 60/226,894, filed Aug. 23, 2000 and its corresponding utility application Ser. No. 09/726,220, filed Nov. 28, 2000, both entitled "Graphics Processing System With Enhanced Memory Controller";

provisional application No. 60/226,914, filed Aug. 23, 2000 and its corresponding utility application Ser. No. 09/722,390, filed Nov. 28, 2000, both entitled "Low Cost Graphics System With Stitching Hardware Support For Skeletal Animation", and

provisional application No. 60/227,006, filed Aug. 23, 2000 and its corresponding utility application Ser. No. 09/722,421, filed Nov. 28, 2000, both entitled "Shadow Mapping In A Low Cost Graphics System".

FIELD OF THE INVENTION

The present invention relates to computer graphics, and more particularly to interactive graphics systems such as home video game platforms. Still more particularly this invention relates to Z-value clamping in the near-Z range when rendering anti-aliased scenes to maximize precision of visually important Z components and to avoid near-Z clipping.

BACKGROUND AND SUMMARY OF THE INVENTION

Many of us have seen films containing remarkably realistic dinosaurs, aliens, animated toys and other fanciful creatures. Such animations are made possible by computer graphics. Using such techniques, a computer graphics artist can specify how each object should look and how it should change in appearance over time, and a computer then models the objects and displays them on a display such as your television or a computer screen. The computer takes care of performing the many tasks required to make sure that each part of the displayed image is colored and shaped just right based on the position and orientation of each object in a scene, the direction in which light seems to strike each object, the surface texture of each object, and other factors.

Because computer graphics generation is complex, computer-generated three-dimensional graphics just a few years ago were mostly limited to expensive specialized flight simulators, high-end graphics workstations and supercomputers. The public saw some of the images generated by these computer systems in movies and expensive television advertisements, but most of us couldn't actually interact with the computers doing the graphics generation. All this has changed with the availability of relatively inexpensive 3D graphics platforms such as, for example, the Nintendo 64® and various 3D graphics cards now available for personal computers. It is now possible to interact with exciting 3D animations and simulations on relatively inexpensive computer graphics systems in your home or office.

Most 3D graphics computer systems render and prepare images for display in response to polygon vertex attribute data which typically includes a Z-axis (scene depth) value. A well known technique called Z-buffering is often used to properly render objects in accordance with their respective depth (i.e., distance from the viewer/camera) in a 3D scene. Since processing a lot of 3D image polygon vertex attribute data can become very time consuming, graphics system designers often employ a polygon culling and clipping process to eliminate the processing of the non-displayed image data. This non-displayed image data is typically polygon vertex data that is outside a viewing frustum bounded by predetermined "clipping" planes in a virtual 3D image rendering space called "camera space" (also called "screen space"). For example, portions of a 3D scene or object that are behind the camera (viewport) position need not be rendered and may be culled or clipped. Likewise, scene portions and 3D objects very far in the scene distance (i.e., far from the camera/eye position along the scene depth or Z-axis) need not be rendered.

Scene depth clipping may be performed using both a near clipping plane and a far clipping plane where the far clipping plane is many times the depth of the near clipping plane. Scene depth clipping may also be performed with a clipping plane at or behind the camera/eye position (i.e., the Z=0 plane) or without using a near clipping plane altogether. However, for various reasons not discussed in detail here, rendering 3D objects at or very close to the camera/eye position may cause certain data processing problems such as overflow and wrapping errors due to the small Z values involved. For example, in the case of geometry projection, vertices that get "too close" to the camera (Z=0) plane get a w (homogeneous coordinate scale factor) value that is very small. Dividing vertex x, y and z coordinates attributes by such small w values during screen-space transformation operations often causes precision and overflow problems-especially when w=0, where the resulting scale values are infinite. Clipping geometry to a near-plane avoids such problems—each triangle with offending vertices is cut into pieces by the near-plane, and the half that is 'too close' is thrown away. Consequently, if scene depth clipping is performed using a near clipping plane in front of the camera/eye

position, the near clipping plane should be positioned far enough in front of the camera that such overflow and wrapping errors do not occur.

Alternatively, if scene depth clipping is performed without using a near clipping plane, or with a clipping plane at or behind the camera/eye position, it may be necessary to burden the applications program with the responsibility of preventing such overflows and wrapping problems by policing the permissible distance between the camera position and a rendered object. A problem graphics system designers confronted in the past is how to avoid certain undesirable visual effects associated with the clipping of polygons of a displayed 3D image object that approaches the plane of the viewer (i.e., the camera/eye plane). In particular, graphics artists and game developers never want to see a 3D object clipped by a clipping plane placed in front of the viewer, as this produces a hole in the object and gives the appearance that objects are hollow. One solution is to define a six plane viewing frustrum clipping box having the near clipping plane very close to the eye/camera plane (i.e., the Z=0 plane) and establish an application program rule that no 3D animated objects should come closer to the eye/camera plane than the near clipping plane. With the near clipping plane placed very close to the eye/camera plane, it less likely that objects that need to be rendered somewhat near the eye/camera plane will come so close as to suffer the ill effects of clipping. Unfortunately, placing the near clipping plane very close to the eye/camera plane reduces the Z depth precision towards the far clipping plane. This Z precision problem is particularly exacerbated when only a limited number of Z-buffer bits are available for depth precision. The less bits that are available for representing a Z value, the greater the precision problem.

If performing Z-buffering in a graphics system where a large number a bits, for example, 24 bits or more, are available in the hardware for representing Z-axis depth values, Z value precision may not pose a problem. However, in certain systems or implementations where less bits are available for representing Z-axis depth values, lack of sufficient Z value precision can seriously effect Z-buffering performance and accuracy. For example, in certain implementations it may be desirable to perform data compression to accommodate storage memory constraints. If Z data compression is performed, the degree of Z precision for providing accurate Z-buffering may be adversely affected.

The present invention also solves the above problems by providing techniques and arrangements in a 3D graphics rendering system for preserving Z value depth precision when performing Z-buffering where the Z value depth data must be compressed.

The present invention also solves the above problems by providing techniques and arrangements in a 3D graphics rendering system for allowing a Z-clipping plane to be used very close to the eye/camera plane—to avoid undesirable visual artifacts produced when objects are rendered too near to the eye/camera plane—while preserving Z value depth precision.

The present invention also solves the above problems by providing techniques and arrangements in a 3D graphics rendering system for performing Z-buffering where the Z depth value associated with a polygon vertex is represented using, for example, 23 bits or less.

More specifically, in an exemplary embodiment of the present invention, a Z-clamping arrangement is employed to improve the precision of visually important Z components by providing Z value clamping within a predetermined range of the Z=0 eye/camera (viewport) plane. This arrangement allows a Z-clipping plane to be used very close to the eye/camera plane—to avoid undesirable visual artifacts produced when objects rendered near to the eye/camera plane are clipped-while preserving Z precision. A near clipping plane, “znear”, is established at a Z plane very close to the Z=0 plane and a far clipping plane, “z-far”, is established at a Z plane far from the Z=0 plane. A clamping plane, “znear**2**”, is then established such that it is located at Z=znear * (1<<n), where n is an integer that effectively determines the Z resolution for the scene by setting the position of the znear**2** plane relative to the znear plane. Z-buffering is performed for all pixels that lie within a range between the znear**2** plane and the z-far clipping plane. Any pixels that lie within the range between the znear plane and znear**2** plane have Z values clamped, for example, to zero or to the Z value of the clamping plane. Hardware geometry clipping is performed for all pixels where z<znear.

In an example implementation, a conventional Z value compression circuit provided in the graphics pipeline is enhanced to perform Z-clamping within the predetermined range of Z values. The enhanced circuitry includes an adder for left-shifting the Z value one or more bits prior to compression and gates for masking out the most significant non-zero shifted bits to zero.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other features and advantages provided by the invention will be better and more completely understood by referring to the following detailed description of presently preferred embodiments in conjunction with the drawings, of which:

FIG. **1** is an overall view of an example interactive computer graphics system;

FIG. **2** is a block diagram of the FIG. **1** example computer graphics system;

FIG. **3** is a block diagram of the example graphics and audio processor shown in FIG. **2**;

FIG. **4** is a block diagram of the example 3D graphics processor shown in FIG. **3**;

FIG. **5** is an example logical flow diagram of the FIG. **4** graphics and audio processor;

FIG. **6** is a flow chart illustrating example steps for implementing Z-clamping in the near Z range in accordance with the present invention;

FIG. **7** is a diagram illustrating in screen space the near-Z clamping arrangement of the present invention;

FIG. **8**A is an example hardware logic diagram for implementing Z compression in the graphics pipeline embodiment of the present invention;

FIG. **8**B is a hardware logic diagram for implementing an example near-Z clamping arrangement in the graphics pipeline embodiment of the present invention; and

FIGS. **9** and **10** show example alternative compatible implementations.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS OF THE INVENTION

FIG. **1** shows an example interactive 3D computer graphics system **50**. System **50** can be used to play interactive 3D video games with interesting stereo sound. It can also be used for a variety of other applications.

In this example, system **50** is capable of processing, interactively in real time, a digital representation or model of a three-dimensional world. System **50** can display some or all of the world from any arbitrary viewpoint. For example, system **50** can interactively change the viewpoint in response to real time inputs from handheld controllers **52***a*, **52***b* or other input devices. This allows the game player to see the world through the eyes of someone within or outside of the world. System **50** can be used for applications that do not require real time 3D interactive display (e.g., 2D display generation and/or non-interactive display), but the capability of displaying quality 3D images very quickly can be used to create very realistic and exciting game play or other graphical interactions.

To play a video game or other application using system, the user first connects a main unit **54** to his or her color television set **56** or other display device by connecting a cable **58** between the two. Main unit **54** produces both video signals and audio signals for controlling color television set **56**. The video signals are what controls the images displayed on the television screen **59**, and the audio signals are played back as sound through television stereo loudspeakers **61**L, **61**R.

The user also needs to connect main unit **54** to a power source. This power source may be a conventional AC adapter (not shown) that plugs into a standard home electrical wall socket and converts the house current into a lower DC voltage signal suitable for powering the main unit **54**. Batteries could be used in other implementations.

The user may use hand controllers **52***a*, **52***b* to control main unit **54**. Controls **60** can be used, for example, to specify the direction (up or down, left or right, closer or further away) that a character displayed on television **56** should move within a 3D world. Controls **60** also provide input for other applications (e.g., menu selection, pointer/cursor control, etc.). Controllers **52** can take a variety of forms. In this example, controllers **52** shown each include controls **60** such as joysticks, push buttons and/or directional switches. Controllers **52** may be connected to main unit **54** by cables or wirelessly via electromagnetic (e.g., radio or infrared) waves.

To play an application such as a game, the user selects an appropriate storage medium **62** storing the video game or other application he or she wants to play, and inserts that storage medium into a slot **64** in main unit **54**. Storage medium **62** may, for example, be a specially encoded and/or encrypted optical and/or magnetic disk. The user may operate a power switch **66** to turn on main unit **54** and cause the main unit to begin running the video game or other application based on the software stored in the storage medium **62**. The user may operate controllers **52** to provide inputs to main unit **54**. For example, operating a control **60** may cause the game or other application to start. Moving other controls **60** can cause animated characters to move in different directions or change the user’s point of view in a 3D world. Depending upon the particular software stored within the storage medium **62**, the various controls **60** on the controller **52** can perform different functions at different times.

Example Electronics of Overall System

FIG. **2** shows a block diagram of example components of system.

The Primary Components Include:

a main processor (CPU) **110**,

a main memory **112**, and

a graphics and audio processor **114**.

In this example, main processor **110** (e.g., an enhanced IBM Power PC 750) receives inputs from handheld controllers **108** (and/or other input devices) via graphics and audio processor **114**. Main processor **110** interactively responds to user inputs, and executes a video game or other program supplied, for example, by external storage media **62** via a mass storage access device **106** such as an optical disk drive. As one example, in the context of video game play, main processor **110** can perform collision detection and animation processing in addition to a variety of interactive and control functions.

In this example, main processor **110** generates 3D graphics and audio commands and sends them to graphics and audio processor **114**. The graphics and audio processor **114** processes these commands to generate interesting visual images on display **59** and interesting stereo sound on stereo loudspeakers **61**R, **61**L or other suitable sound-generating devices.

Example system includes a video encoder **120** that receives image signals from graphics and audio processor **114** and converts the image signals into analog and/or digital video signals suitable for display on a standard display device such as a computer monitor or home color television set **56**. System **50** also includes an audio codec (compressor/decompressor) **122** that compresses and decompresses digitized audio signals and may also convert between digital and analog audio signaling formats as needed. Audio codec **122** can receive audio inputs via a buffer **124** and provide them to graphics and audio processor **114** for processing (e.g., mixing with other audio signals the processor generates and/or receives via a streaming audio output of mass storage access device **106**). Graphics and audio processor **114** in this example can store audio related information in an audio memory **126** that is available for audio tasks. Graphics and audio processor **114** provides the resulting audio output signals to audio codec **122** for decompression and conversion to analog signals (e.g., via buffer amplifiers **128**L, **128**R) so they can be reproduced by loudspeakers **61**L, **61**R.

Graphics and audio processor **114** has the ability to communicate with various additional devices that may be present within system **50**. For example, a parallel digital bus **130** may be used to communicate with mass storage access device **106** and/or other components. A serial peripheral bus **132** may communicate with a variety of peripheral or other devices including, for example:

a programmable read-only memory and/or real time clock **134**,

a modem **136** or other networking interface (which may in turn connect system **50** to a telecommunications network **138** such as the Internet or other digital network from/to which program instructions and/or data can be downloaded or uploaded), and

flash memory **140**.

A further external serial bus **142** may be used to communicate with additional expansion memory **144** (e.g., a memory card) or other devices. Connectors may be used to connect various devices to busses **130**, **132**, **142**.

Example Graphics And Audio Processor

FIG. **3** is a block diagram of an example graphics and audio processor **114**. Graphics and audio processor **114** in one example may be a single-chip ASIC (application specific integrated circuit). In this example, graphics and audio processor **114** includes:

a processor interface **150**,

a memory interface/controller **152**,

a 3D graphics processor **154**,

an audio digital signal processor (DSP) **156**,

an audio memory interface **158**,

an audio interface and mixer **160**,

a peripheral controller **162**, and

a display controller **164**.

3D graphics processor **154** performs graphics processing tasks. Audio digital signal processor **156** performs audio processing tasks. Display controller **164** accesses image information from main memory **112** and provides it to video encoder **120** for display on display device **56**. Audio interface and mixer **160** interfaces with audio codec **122**, and can also mix audio from different sources (e.g., streaming audio from mass storage access device **106**, the output of audio DSP **156**, and external audio input received via audio codec **122**). Processor interface **150** provides a data and control interface between main processor **110** and graphics and audio processor **114**.

Memory interface **152** provides a data and control interface between graphics and audio processor **114** and memory **112**. In this example, main processor **110** accesses main memory **112** via processor interface **150** and memory interface **152** that are part of graphics and audio processor **114**. Peripheral controller **162** provides a data and control interface between graphics and audio processor **114** and the various peripherals mentioned above. Audio memory interface **158** provides an interface with audio memory **126**.

Example Graphics Pipeline

FIG. **4** shows a more detailed view of an example 3D graphics processor **154**. 3D graphics processor **154** includes, among other things, a command processor **200** and a 3D graphics pipeline **180**. Main processor **10** communicates streams of data (e.g., graphics command streams and display lists) to command processor **200**. Main processor **110** has a two-level cache **115** to minimize memory latency, and also has a write-gathering buffer **111** for un-cached data streams targeted for the graphics and audio processor **114**. The write-gathering buffer **111** collects partial cache lines into full cache lines and sends the data out to the graphics and audio processor **114** one cache line at a time for maximum bus usage.

Command processor **200** receives display commands from main processor **110** and parses them—obtaining any additional data necessary to process them from shared memory **112**. The command processor **200** provides a stream of vertex commands to graphics pipeline **180** for 2D and/or 3D processing and rendering. Graphics pipeline **180** generates images based on these commands. The resulting image information may be transferred to main memory **112** for access by display controller/video interface unit **164**—which displays the frame buffer output of pipeline **180** on display **56**.

FIG. **5** is a logical flow diagram of graphics processor **154**. Main processor **110** may store graphics command streams **210**, display lists **212** and vertex arrays **214** in main memory **112**, and pass pointers to command processor **200** via bus interface **150**. The main processor **110** stores graphics commands in one or more graphics first-in-first-out (FIFO) buffers **210** it allocates in main memory **110**. The command processor **200** fetches:

command streams from main memory **112** via an on-chip FIFO memory buffer **216** that receives and buffers the graphics commands for synchronization/flow control and load balancing,

display lists **212** from main memory **112** via an on-chip call FIFO memory buffer **218**, and

vertex attributes from the command stream and/or from vertex arrays **214** in main memory **112** via a vertex cache **220**.

Command processor **200** performs command processing operations **200***a* that convert attribute types to floating point format, and pass the resulting complete vertex polygon data to graphics pipeline **180** for rendering/rasterization. A programmable memory arbitration circuitry **130** (see FIG. **4**) arbitrates access to shared main memory **112** between graphics pipeline **180**, command processor **200** and display controller/video interface unit **164**.

FIG. **4** shows that graphics pipeline **180** may include:

a transform unit **300**,

a setup/rasterizer **400**,

a texture unit **500**,

a texture environment unit **600**, and

a pixel engine **700**.

Transform unit **300** performs a variety of 2D and 3D transform and other operations **300***a* (see FIG. **5**). Transform unit **300** may include one or more matrix memories **300***b* for storing matrices used in transformation processing **300***a*. Transform unit **300** transforms incoming geometry per vertex from object space to screen space; and transforms incoming texture coordinates and computes projective texture coordinates (**300***c*). Transform unit **300** performs polygon clipping/culling (**300***d*). Lighting processing **300***e*, also performed by transform unit **300**, provides per vertex lighting computations for up to eight independent lights in one example embodiment. Transform unit **300** may also perform texture coordinate generation (**300***c*) for emboss-style bump mapping effects. Also, as discussed later herein in greater detail, Transform unit **300** performs depth (Z value) compression and clamping.

Setup/rasterizer **400** includes a setup unit which receives vertex data from transform unit **300** and sends triangle setup information to one or more rasterizer units (**400***b*) performing edge rasterization, texture coordinate rasterization and color rasterization.

Texture unit **500** (which may include an on-chip texture memory (TMEM) **502**) performs various tasks related to texturing including for example:

retrieving textures **504** from main memory **112**,

texture processing (**500***a*) including, for example, multi-texture handling, post-cache texture decompression, texture filtering, embossing, shadows and lighting through the use of projective textures, and BLIT with alpha transparency and depth,

bump map processing for computing texture coordinate displacements for bump mapping, pseudo texture and texture tiling effects (**500***b*), and

indirect texture processing (**500***c*).

Texture unit **500** performs texture processing using both regular (non-indirect) and indirect texture lookup operations. A more detailed description of the example graphics pipeline circuitry and procedures for performing regular and indirect texture look-up operations is disclosed in commonly assigned co-pending patent application, Ser. No. 09/722,382, entitled "Method And Apparatus For Direct And Indirect Texture Processing In A Graphics System" and its corresponding provisional application, Ser. No. 60/226,891, filed Aug. 23, 2000, both of which are incorporated herein by reference.

Texture unit **500** outputs filtered texture values to the Texture Environment Unit **600** for texture environment processing (**600***a*). Texture environment unit **600** blends polygon and texture color/alpha/depth, and can also perform texture fog processing (**600***b*) to achieve inverse range based fog effects. Texture environment unit **600** can provide multiple stages to perform a variety of other interesting environment-related functions based for example on color/alpha modulation, embossing, detail texturing, texture swapping, clamping, and depth blending. Texture environment unit **600** can also combine (e.g., subtract) textures in hardware in one pass. For more details concerning the texture environment unit **600**, see commonly assigned application Ser. No. 09/722,367 entitled "Recirculating Shade Tree Blender for a Graphics System" and its corresponding provisional application, No. 60/226,888, filed Aug. 23, 2000, both of which are incorporated herein by reference.

Pixel engine **700** performs depth (Z value) compare (**700***a*) and pixel blending (**700***b*). In this example, pixel engine **700** stores data into an embedded (on-chip) frame buffer memory **702**. Graphics pipeline **180** may include one or more embedded DRAM memories **702** to store frame buffer and/or texture information locally. Z value depth compares **700***a*' can also be performed at an earlier stage in the graphics pipeline **180** depending on the rendering mode currently in effect (e.g., Z value compares can be performed earlier if alpha blending is not required). The pixel engine **700** includes a copy operation **700***c* that periodically writes on-chip frame buffer **702** to main memory **112** for access by display/video interface unit **164**. This copy operation **700***c* can also be used to copy embedded frame buffer **702** contents to textures in the main memory **112** for dynamic texture synthesis effects.

In this example graphics system, Anti-aliasing and other filtering can be also performed during the copy-out operation. For more details concerning anti-aliasing see provisional application No. 60/226,900, filed Aug. 23, 2000 and its corresponding utility application Ser. No. 09/726,226, filed Nov. 28, 2000, both entitled "Method And Apparatus For Anti-Aliasing In A Graphics System", both of which are incorporated herein by reference.

The frame buffer output of graphics pipeline **180** (which is ultimately stored in main memory **112**) is read each frame by display/video interface unit **164**. Display controller/video interface **164** provides digital RGB pixel values for display on display **102**.

Example Z-Clamping Arrangement

A Z-clamping arrangement is used to improve the precision of the visually important Z-axis (depth) attributes of rendered scene components by clamping to zero the Z value of pixels that fall within a predetermined range in front of the eye/camera (viewport) plane at Z=0. FIG. **6** illustrates an example of the Z value clamping arrangement of the present invention as viewed in screen space. A Z-clipping plane **201**, "znear", is defined very close to the Z=0 eye/camera plane **202**, so as to avoid undesirable visual artifacts produced when objects are rendered too near to the eye/camera plane. A clamping plane **203**, "znear2", is established such that znear2 is located at a Z plane equal to znear*(1<<n), where n is an integer that effectively determines the Z resolution for the scene by setting the position of the znear2 plane relative to the znear plane. A far clipping plane **204**, "zfar", is also established at a Z plane far from the Z=0 plane. Z-buffering is performed for all pixels that lie within a range between the znear2 plane and the z-far clipping plane. Any pixels that lie within the range between the znear plane and znear2 plane have Z values clamped, for example, to zero (or to some minimum Z value such as the Z value of the znear2 clamping plane) and normal clipping is performed on geometry for all pixels where z<znear.

FIG. **7** shows a flowchart of an example set of general processing steps **301** for obtaining improved Z precision when implementing Z-buffering in a graphics processing system. A "Z" depth value is generally computed or provided to the graphics rendering system as an polygon vertex attribute, as indicated at block **302**. In the Z-clamping method of the present invention, a clipping plane "znear" is established at a Z axis plane very close to the Z=0 plane and another clipping plane "zfar" is established at Z axis position far from the Z=0 plane, as indicated at block **304**. A clamping plane "znear**2**" is also established, as indicated at block **306**, at a Z axis plane where Z=znear**2**=znear * (1<<n), where n is an integer that effectively determines the Z resolution for the scene by setting the position of the znear**2** plane relative to the near znear plane (i.e., the farther the znear**2** plane is positioned from the znear plane, the greater the Z-buffering resolution available for that portion of the rendered scene that is farther from the camera/eye plane than the znear**2** plane). Normal Z-buffering is performed for all pixels having Z values where znear**2**<Z<zfar, as indicated at block **308**. For pixels having Z values equal to or between the znear and the znear**2** clamping planes (i.e., where znear≦Z≦znear**2**), the Z value is clamped (e.g., clamped to zero or to a minimum value such as the value of the znear**2** plane) and the corresponding pixels are written to the frame buffer in a first-to-last order, as indicated in block **310**. For pixels where Z<znear, conventional geometry clipping is performed, as indicated at block **312**. In the example graphics pipeline embodiment, most of the FIG. **7** steps are performed by clipping logic and an enhanced Z-compression logic in Transform Unit **300**, as described in the example hardware implementation below.

Example Hardware Implementation

In example graphics pipeline **180**, Transform Unit **300** includes both clipping plane logic circuitry and Z-compression logic circuitry. Because processing anti-aliased pixels requires more data to be stored in a limited size Z-buffer (i.e., embedded Frame Buffer **702**), the Z value compression is performed in this example embodiment only when full scene anti-aliasing is enabled. Such Z-compression circuitry normally operates to compress a computed 24 bit Z attribute value to a 16 bit value. FIG. **8A** shows example hardware logic circuitry that may be used for providing Z compression without providing any clamping of Z values. This example Z compression circuit essentially comprises a priority encoder **320** and a shifter **322** which performs compression on four 24 bit Z values, converting them to 16 bit values.

In the example implementation of graphics pipeline **180**, a compression algorithm performs a type of reverse floating point encoding. Whereas conventional floating point notation clumps most of the resolution towards the lower end of the number scale, the properties of screen-space Z necessitate providing most of the resolution towards the upper end of the number scale. To accomplish such, three compression schemes are used, with a selection between the three schemes being based on the particular near-to-far ratio used in the rendered scene. For example, when using orthographic projection or small far-to-near ratios, a direct linear compression mapping is used wherein the lower eight bits are simply stripped from the input Z value. For medium far-to-near ratios, a floating point conversion to 16 bits using **14**e**2** notation is used to represent a 24 bit Z value. This form of compression provides an effective 15 bit resolution bits at the near plane and a 17 bit resolution at the far plane. For high far-to-near ratios, a floating point conversion to 16 bits using **13**e**3** notation is used to represent the 24 bit Z value. This has an effective resolution of 14 bits at the near plane and 20 bits at the far plane.

One straight forward simple implementation of the above floating point conversion approach to compression involves selecting an exponent and a shift value, then shifting the input value down by an amount of the shift value and appending the exponent at the high order bit position. In the example embodiment, an exponent and shift value are chosen by detecting the particular range of values within which the upper bits of an input Z value fall, as indicated by the following tables:

For 14e2 notation compression:

z [23:21]	exp	shift
000-011	0	9
100-101	1	8
110-110	2	7
111-111	3	7

For 13e3 notation compression:

z [23:17]	exp	shift
0000000-0111111	0	10
1000000-1011111	1	9
1100000-1101111	2	8
1110000-1110111	3	7
1111000-1111011	4	6
1111100-1111101	5	5
1111110-1111110	6	4
1111111-1111111	7	4

In the present example, Transform Unit **300** may use conventional hardware clipping circuitry for programmably setting and providing Z near and Z far clipping planes (as well as appropriate X and Y axis clipping planes). To implement the Z-clamping arrangement and setting a Z-clamping plane as described above, Transform Unit **300** uses an enhanced Z-compression logic circuitry as shown in FIG. **8**B. In addition to the shifting of bits that is associated with Z value compression, this circuit allows additional shifting of one or more of the most significant bits (MSBs) of the input Z value to be performed when implementing one of the above two floating point conversion compression schemes. As shown in FIG. **8**B, this enhanced circuit arrangement uses a priority encoder **320**, a 4-bit (or smaller) adder **324** and a shifter **322**, plus AND gates (not shown) for masking the most significant Z-value bits. The shifting of the pre-compressed input Z value is determined by programmable adder **324**, where "n" represents the number of additional bit position shifts to be performed.

Other Example Compatible Implementations

Certain of the above-described system components **50** could be implemented as other than the home video game console configuration described above. For example, one could run graphics application or other software written for system **50** on a platform with a different configuration that emulates system **50** or is otherwise compatible with it. If the other platform can successfully emulate, simulate and/or provide some or all of the hardware and software resources of system **50**, then the other platform will be able to successfully execute the software.

As one example, an emulator may provide a hardware and/or software configuration (platform) that is different from the hardware and/or software configuration (platform) of system **50**. The emulator system might include software and/or hardware components that emulate or simulate some or all of hardware and/or software components of the system for which the application software was written. For example, the emulator system could comprise a general purpose digital computer such as a personal computer, which executes a software emulator program that simulates the hardware and/or firmware of system **50**.

Some general purpose digital computers (e.g., IBM or MacIntosh personal computers and compatibles) are now equipped with 3D graphics cards that provide 3D graphics pipelines compliant with DirectX or other standard 3D graphics command APIs. They may also be equipped with stereophonic sound cards that provide high quality stereophonic sound based on a standard set of sound commands. Such multimedia-hardware-equipped personal computers running emulator software may have sufficient performance to approximate the graphics and sound performance of system **50**. Emulator software controls the hardware resources on the personal computer platform to simulate the processing, 3D graphics, sound, peripheral and other capabilities of the home video game console platform for which the game programmer wrote the game software.

FIG. **9** illustrates an example overall emulation process using a host platform **1201**, an emulator component **1303**, and a game software executable binary image provided on a storage medium **62**. Host **1201** may be a general or special purpose digital computing device such as, for example, a personal computer, a video game console, or any other platform with sufficient computing power. Emulator **1303** may be software and/or hardware that runs on host platform **1201**, and provides a real-time conversion of commands, data and other information from storage medium **62** into a form that can be processed by host **1201**. For example, emulator **1303** fetches "source" binary-image program instructions intended for execution by system from storage medium **62** and converts these program instructions to a target format that can be executed or otherwise processed by host **1201**.

As one example, in the case where the software is written for execution on a platform using an IBM PowerPC or other specific processor and the host **1201** is a personal computer using a different (e.g., Intel) processor, emulator **1303** fetches one or a sequence of binary-image program instructions from storage medium **62** and converts these program instructions to one or more equivalent Intel binary-image program instructions. The emulator **1303** also fetches and/or generates graphics commands and audio commands intended for processing by the graphics and audio processor **114**, and converts these commands into a format or formats that can be processed by hardware and/or software graphics and audio processing resources available on host **1201**. As one example, emulator **1303** may convert these commands into commands that can be processed by specific graphics and/or or sound hardware of the host **1201** (e.g., using standard DirectX, OpenGL and/or sound APIs).

An emulator **1303** used to provide some or all of the features of the video game system described above may also be provided with a graphic user interface (GUI) that simplifies or automates the selection of various options and screen modes for games run using the emulator. In one example, such an emulator **1303** may further include enhanced functionality as compared with the host platform for which the software was originally intended. In the case where particular graphics support hardware within an emulator does not include the near-z processing functions shown in FIGS. **7** and **8**, the emulator designer has a choice of either:

implementing the near-z processing functions in software with a potential corresponding decrease in performance depending upon the speed of the processor, or

"stubbing" (i.e., ignoring) the near-z processing to provide a rendered image that may have near image artifacts.

While the FIG. **6** flowchart may be implemented entirely in software, entirely in hardware or by a combination of hardware and software, the preferred embodiment performs most of these calculations in hardware to obtain increased speed performance and other advantages. Nevertheless, in other implementations (e.g., where a very fast processor is available), the computations and steps of FIG. **6** may be implemented in software to provide similar or identical imaging results.

FIG. **10** illustrates an emulation host system **1201** suitable for use with emulator **1303**. System **1201** includes a processing unit **1203** and a system memory **1205**. A system bus **1207** couples various system components including system memory **1205** to processing unit **1203**. System bus **1207** may be any of several types of bus structures including a memory bus or memory controller, a peripheral bus, and a local bus using any of a variety of bus architectures. System memory **1207** includes read only memory (ROM) **1252** and random access memory (RAM) **1254**. A basic input/output system (BIOS) **1256**, containing the basic routines that help to transfer information between elements within personal computer system **1201**, such as during start-up, is stored in the ROM **1252**. System **1201** further includes various drives and associated computer-readable media. A hard disk drive **1209** reads from and writes to a (typically fixed) magnetic hard disk **1211**. An additional (possible optional) magnetic disk drive **1213** reads from and writes to a removable "floppy" or other magnetic disk **1215**. An optical disk drive **1217** reads from and, in some configurations, writes to a removable optical disk **1219** such as a CD ROM or other optical media. Hard disk drive **1209** and optical disk drive **1217** are connected to system bus **1207** by a hard disk drive interface **1221** and an optical drive interface **1225**, respectively. The drives and their associated computer-readable media provide nonvolatile storage of computer-readable instructions, data structures, program modules, game programs and other data for personal computer system **1201**. In other configurations, other types of computer-readable media that can store data that is accessible by a computer (e.g., magnetic cassettes, flash memory cards, digital video disks, Bernoulli cartridges, random access memories (RAMs), read only memories (ROMs) and the like) may also be used.

A number of program modules including emulator **1303** may be stored on the hard disk **1211**, removable magnetic disk **1215**, optical disk **1219** and/or the ROM **1252** and/or the RAM **1254** of system memory **1205**. Such program modules may include an operating system providing graphics and sound APIs, one or more application programs, other program modules, program data and game data. A user may enter commands and information into personal computer system **1201** through input devices such as a keyboard **1227**, pointing device **1229**, microphones, joysticks, game controllers, satellite dishes, scanners, or the like. These and other input devices can be connected to processing unit **1203** through a serial port interface **1231** that is coupled to system bus **1207**, but may be connected by other interfaces, such as a parallel port, game port Fire wire bus or a universal serial bus (USB). A monitor **1233** or other type of display device is also connected to system bus **1207** via an interface, such as a video adapter **1235**.

System **1201** may also include a modem **1154** or other network interface means for establishing communications over a network **1152** such as the Internet. Modem **1154**, which may be internal or external, is connected to system bus **123** via serial port interface **1231**. A network interface **1156** may also be provided for allowing system **1201** to communicate with a remote computing device **1150** (e.g., another system **1201**) via a local area network **1158** (or such communication may be via wide area network **1152** or other communications path such as dial-up or other communications means). System **1201** will typically include other peripheral output devices, such as printers and other standard peripheral devices.

In one example, video adapter **1235** may include a 3D graphics pipeline chip set providing fast 3D graphics rendering in response to 3D graphics commands issued based on a standard 3D graphics application programmer interface such as Microsoft's DirectX 7.0 or other version. A set of stereo loudspeakers **1237** is also connected to system bus **1207** via a sound generating interface such as a conventional "sound card" providing hardware and embedded software support for generating high quality stereophonic sound based on sound commands provided by bus **1207**. These hardware capabilities allow system **1201** to provide sufficient graphics and sound speed performance to play software stored in storage medium **62**.

All documents referenced above are hereby incorporated by reference.

While the invention has been described in connection with what is presently considered to be the most practical and preferred embodiment, it is to be understood that the invention is not to be limited to the disclosed embodiment, but on the contrary, is intended to cover various modifications and equivalent arrangements included within the scope of the appended claims.

We claim:

1. In a 3D graphics rendering system, a method of performing Z buffering, comprising:

establishing a first clipping plane, znear, at a Z-axis position very near to the Z=0 plane and a second clipping plane, zfar, at a Z-axis position very far from the z=0 plane;

establishing a Z-axis value clamping plane, znear**2**, at z=znear**2**=znear*(1<<n), wherein "n" is a predetermined integer value that sets a position of the znear**2** clamping plane relative to the znear plane and effectively provides a predetermined z value resolution for a portion of a rendered scene that lies between the znear**2** plane and the zfar plane;

performing conventional Z-buffering for pixels having z values where znear**2**<z<zfar; and

clamping z values to a predetermined value for pixels where znear≦z≦znear**2**, wherein pixel data corresponding to clamped z values is written to a display frame buffer in a first to last rendered order.

2. The graphics system of claim **1** wherein the predetermined value for clamped Z values is zero.

3. In a 3D graphics rendering system including a processor and a separate graphics processing pipeline having transformation and lighting circuitry, the pipeline performing Z buffering, an arrangement included within the graphics pipeline for providing Z value compression and selectable Z value clamping, comprising:

a priority encoder and a shifter, wherein said priority encoder provides a shift value to said shifter for performing a binary value compression operation; and

an adder including bit masking circuitry, said adder connected between the priority encoder and the shifter,

wherein said adder is used to selectably increase a shift value provided by the priority encoder to said shifter during a Z value compression operation to effectively clamp Z values within a selectable predetermined range.

4. The graphics system of claim **3** wherein said predetermined Z value is zero.

5. The graphics system of claim **3** wherein said predetermined range of Z values is determined by a Z clipping plane, znear, defined at a predetermined Z-axis position very near to the z=0 plane and a Z clamping plane, znear**2**, defined at z=znear**2**=znear*(1<<n), where "n" is equal to an integer value indicative of a selected increase in shift value provided to said priority encoder.

6. In a 3D graphics rendering system including a processor and a separate graphics processing pipeline, the pipeline performing full scene anti-aliasing with Z-value compression, a method for selectably setting a predetermined Z value resolution for a portion of a rendered scene, comprising:

shifting a binary Z-value one or more bit positions prior to performing Z value compression, wherein the amount of shifting determines a range of Z values near a Z=0 plane for which Z values are clamped to a predetermined value.

7. In a graphics processing system that renders and displays images at least in part in response to polygon vertex attribute data including Z-value binary data stored in an associated memory, a Z value compression processing circuit portion embodied in hardware, comprising:

a priority encoder,

a shifter, and

an adder connected between the priority encoder and the shifter, wherein the adder may be used to selectably increase a value provided by said priority encoder to said shifter for shifting the Z-value binary data an additional predetermined number of bit positions during a compression operation to effectuate a clamping of Z values that are within a predetermined range of Z values to a predetermined value.

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